Test Report No. G231-2890

No. of Pages 90

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9/p

Report of Test on

TITLE

SEMICONDUCTORS

TRANSISTORS - DIODES

ACCEPTANCE TESTS

(NASA contract NAS8-2551)

FOR

NATIONAL AERONAUTICS & SPACE ADMINISTRATION

Associated Testing Laboratories, Inc.

Wayne, New Jersey

Date September 28, 1962

o refer

	Prepared	Checked	Approved
By	J. Deppe Jr.	H. Rosenfeld	K. Dambach
Signed	J. Deppe Jr.	H. Rosenfeld	K. Dambach
Date	9-28-62	9-28-62	9-28-62

[redacted]

Enclosure #1

RQT-6961

[redacted]

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Associated Testing Laboratories, Inc.
Wayne, New Jersey Winter Park, Florida
Burlington, Massachusetts

Administrative Data

1.0 Purpose of Test:

The enclosed format includes the Test Procedures which were required to perform the necessary parameter measurements and environmental tests in accordance with National Aeronautics & Space Administration Task No. A8.

2.0 Manufacturer: See individual test reports for vendors submitted in this test program.

3.0 Manufacturer's Type or Model No.: See individual test reports for manufacturers, types or model numbers.

4.0 Drawing, Specification or Exhibit: N.A.S.A. Task Order No. A8, Contract No. NAS8-2551 (Amends A1, A2, A3 and A4) and verbal instructions from an Engineering Representative of National Aeronautics & Space Administration

5.0 Quantity of Items Tested: See individual test reports

6.0 Security Classification of Items: Unclassified

7.0 Date Test Completed: September 24, 1962

8.0 Test Conducted By: **Associated Testing Laboratories, Inc.**

9.0 Disposition of Specimens: Returned to National Aeronautics & Space Administration

10.0 Abstract:

The Acceptance Tests were performed in accordance with the above referenced specifications. Included in this report are the Test Procedures which were utilized to perform the parameter measurements and environmental tests. The results acquired in this test program are included in individual reports identified with the subscripts G231-2890-A, G231-2890-B, G231-2890-C, etc.

INTRODUCTION

For purposes of inventory and safe handling, all units received for testing were serialized consecutively by Associated Testing Laboratories, Inc. and mounted on styrofoam pads which in turn were placed in hand-carry tote boxes.

Prior to conducting any said parameter Measurements or exposing the test specimens to environmental testing, the proposed test methods and equipment list were submitted in conference to the National Aeronautics & Space Administration for approval. Following this approval, the Acceptance Tests were performed in accordance with the previously referenced specifications as described in this Test Procedure.

The in-chamber measurements, where applicable, were performed utilizing especially constructed fixtures for in-chamber measurements. The fixtures were constructed of sheet aluminum 12 inches by 19 inches by 1/4 inch. These fixtures were, in turn, supported 5 inches above the chamber floor by 1/16 inch aluminum stock mounted on the undersides of each test panel to provide protection for the leads connected to the Transistor sockets, as well as to provide the necessary shielding to eliminate stray pickup. Thirty test sockets, manufactured of heat resistant phenolic, were mounted on each test fixture. Separate voltage and current leads were connected to each base, collector and emitter terminal on the sockets to eliminate the possibility of recording the voltage drop in the current handling circuits. The leads, of No. 20 gauge Teflon wire, were cabled together in 8 foot lengths, shielded and terminated with Amphenol Type Blue Ribbon Connectors with the assembly having an insulation resistance greater than 1000 x 1000 megohms. The mates to these connectors were wired to two 5-deck, 25-position stepping switches, which were utilized to switch the voltage and current leads simultaneously through 25 positions. The stepping switch position was indicated on Nixie Read-Out Indicators. The six outputs of the stepping switch circuits were interconnected to the appropriate Transistor test panel or auxiliary test equipment as required for the particular parameter measurement.

In general, when performing tests under operational environment, the above mentioned fixtures were placed within the test chamber, and the cables exited through the access ports within the chamber wall.

INTRODUCTION

(Continued)

The chamber temperatures were controlled by means of two pen cam controllers or preset thermostatic controls. However, to compensate for temperature gradients within the test space, thermocouples were connected to the transistor housings and direct readout was accomplished with a thermocouple bridge.

It should be noted that the Transistors were arranged within the test space so that all test specimens were relatively at the same physical level or temperature plateau. Unless otherwise specified, when the thermocouples reached the specified temperature level, the test specimens were maintained at that temperature for an additional two hours of stabilization prior to performing any said parameter measurements.

The in-chamber measurements were then performed utilizing the aforementioned switching circuits and the Transistor test console. The specific parameter measurements are described in the Test Procedure portion of this report. In addition, it should be noted that at no time during the test sequence was the switching accomplished with bias voltages applied to the Transistor under test.

With the exceptions noted, all semi-conductor units submitted for testing were received in two lots. The test parameter measurements and environmental tests, except where noted, were performed on the first lot submitted. Those samples submitted for testing in the second lot (required to fulfill the specified number of samples for storage and operational life) were subjected to "Pre Life End Point Measurements" only, and then inserted into the life tests. The specific serial numbers of vendors subjected to test parameter measurements, environmental tests and life testing may be seen by referring to the original test data and summary of the test results for the specific vendors.

LIST OF APPARATUS

1. Transistor Test Set, Baird-Atomic, Inc., Model No. KP-2-H
2. Transistor Test Set, Dynatran Electronics, Model No. 200 MC H_{FE}
3. Transistor Curve Tracer, Tektronix, Model No. 575
4. Oscilloscope, Tektronix, Model No. 585
5. Oscilloscope, Tektronix, Model No. 502
6. Oscilloscope, Tektronix, Model No. 502
7. Oscilloscope, Tektronix, Model No. 545A
8. Oscilloscope, Hewlett-Packard, Model No. 150A
9. Amplifier, Hewlett-Packard, Model No. 152B
10. Amplifier, Tektronix, Model No. CA
11. Wide Range Oscillator, Hewlett-Packard, Model No. 202C
12. Wide Range Oscillator, Hewlett-Packard, Model No. 200CD
13. Pulse Generator, Electro-Pulse Inc., Model No. 3450C
14. Pulse Generator, Electro-Pulse Inc., Model No. 3450C
15. Random Noise Generator, General Radio Company, Model No. 1390B
16. Transistor Noise Analyzer, Quan-Tech Laboratories, Model No. 310
17. AC Voltmeter, Hewlett-Packard, Model No. 400H
18. AC Voltmeter, Hewlett-Packard, Model No. 400D
19. AC Voltmeter, Hewlett-Packard, Model No. 400H
20. Digital Voltmeter, Cubic Corporation, Model No. V-51
21. DC Digital Voltmeter, Hewlett-Packard, Model No. 405CR

LIST OF APPARATUS

(Continued)

22. DC Voltmeter, Hewlett-Packard, Model No. 412A
23. DC Voltmeter, Hewlett-Packard, Model No. 412A
24. DC Voltmeter, Hewlett-Packard, Model No. 412A
25. DC Voltmeter, Hewlett-Packard, Model No. 412A
26. DC Voltmeter, Hewlett-Packard, Model No. 412A
27. DC Microvolt Ammeter, Hewlett-Packard, Model No. 425AR
28. DC Microvolt Ammeter, Hewlett-Packard, Model No. 425A
29. DC Microvolt Ammeter, Hewlett-Packard, Model No. 425A
30. DC Millimicro Ammeter, Dynatran Electronics Corp. Model No. 1811-AR
31. Multimeter, AVO Ltd., Model No. 8, Mark II
32. Multimeter, AVO Ltd., Model No. 8, Mark II
33. Multimeter, AVO Ltd., Model No. 8, Mark II
34. DC Power Supply, Electronic Measurements Co., Inc., Model No. 212-AMK
35. DC Power Supply, Electronic Measurements Co., Inc., Model No. 212-AM
36. DC Power Supply, Electronic Measurements Co., Inc., Model No. C612AL
37. DC Power Supply, Electronic Measurements Co., Inc., Model No. 212A/M
38. DC Power Supply, Electronic Measurements Co., Inc., Model No. C621-AM
39. DC Power Supply, Electronic Measurements Co., Inc., Model No. C612AL
40. DC Power Supply, Electronic Measurements Co., Inc., Model No. C614BML

LIST OF APPARATUS

(Continued)

41. DC Power Supply, Lambda Electronics Corp., Model No. 50

42. DC Power Supply, Lambda Electronics Corp., Model No. 26

43. DC Power Supply, Sorenson & Company, Inc., Model No. T50-1.5

44. DC Power Supply, Sorenson & Company, Inc., Model No. T50-1.5

45. DC Power Supply, Opad Electric Company, Model No. KM75B

46. DC Power Supply, Opad Electric Company, Model No. KM75B

47. DC Power Supply, Opad Electric Company, Model No. KM93B

48. DC Power Supply, Opad Electric Company, Model No. KM93B

49. DC Power Supply, Opad Electric Company, Model No. RS20

50. DC Power Supply, Opad Electric Company, Model No. RS20

51. DC Power Supply, Opad Electric Company, Model No. RS20

52. DC Power Supply, Opad Electric Company, Model No. RS20

53. DC Power Supply, Opad Electric Company, Model No. RS20B

54. DC Power Supply, Opad Electric Company, Model No. RS10B

55. DC Power Supply, Quan Tech. Laboratories, Model No. 151B

56. Vernier Caliper, Mauser

57. Micrometer Caliper Set, Starrett Company, Model No. 436

58. High Temperature - Low Temperature Humidity Test Chamber, manufactured by Associated Testing Laboratories, Inc., manufacturing Division, Model No. LHH 25

59. High Temperature - Low Temperature Test Chamber, manufactured by Associated Testing Laboratories, Inc., Manufacturing Division, Model No. 3-LH-15-LC

LIST OF APPARATUS

(Continued)

60. High Temperature - Low Temperature Test Chamber, manufactured by Associated Testing Laboratories, Inc., Manufacturing Division, Model No. 3-LH-15-LC

61. Altitude Chamber, manufactured by Associated Testing Laboratories Inc., Manufacturing Division, Model No. A-4-L

62. Altitude Chamber, Kinney Company, Model No. PW-600

63. High Pressure Chamber, Associated Testing Laboratories, Inc., Manufacturing Division, Model No. PC-300

64. Shock Machine, manufactured by Associated Testing Laboratories, Inc., Manufacturing Division, Model No. ST-15

65. Vibration System consisting of the following: (Vibration Exciter and Control Console), Unholtz-Dickie, Model No. 200 VLG84

66. Hot Plate, Edwin L. Wiegand Co., Model No. ROPH151

It should be noted that the general policy of Associated Testing Laboratories, Inc. for making any electrical readings is as follows:

(1) Wherever possible, instrumentation for taking measurements have accuracies of at least ten times greater than the tolerance of the parameter being measured.

(2) All the test equipment used in conducting these measurements are in the frequency span of calibration during the entire test program. If instrumentation goes beyond the calibration frequency span during the test program, the test program is stopped at a convenient spot and the instruments recalibrated.

ASSOCIATED TESTING LABORATORIES, INC.

Albert F. Erdman

Albert F. Erdman
Vice President - Chief Engineer

SECTION I

Transistor Test Parameter Measurement Procedures

Collector-Base Cut-Off Current (ICBO)

Emitter-Base Cut-Off Current (IEBO)

Collector Reverse Current (ICEO)

Collector-Base Breakdown Voltage (BVCBO)

Emitter-Base Breakdown Voltage (BVEBO)

Collector-Emitter Breakdown Voltage (BVCEO)

Base Emitter Voltage (VBE)

Base Emitter Saturation Voltage (VBE SAT)

Collector Emitter Saturation Voltage (VCE SAT)

DC Collector Saturation Resistance (RCS)

Static Forward Current Transfer Ratio (DC hFE)

Emitter-Base Saturation, Pulse, (VEB SAT)

Collector Saturation, Pulse, (VCE SAT)

Static Forward Current Transfer Ratio (Pulse hFE)

Lower Limiting Voltage (LVCER)

Forward Current Transfer Ratio (hfb)

Small Signal Open Circuit Output Admittance (hob)

Small Signal Open Circuit
Reverse Transfer Voltage Ratio (hrb)

Small Signal Short Circuit Input Impedance (hib)

Small Signal Short Circuit Input Impedance (hie)

Small Signal Open Circuit Output Admittance (hoe)

Small Signal Short Circuit Forward Current
Transfer Ratio (hfe @ IKC)

Small Signal Forward Current Transfer Ratio
(hfe @ 1 MC)

SECTION I

Transistor Test Parameter Measurement Procedures

(Continued)

Small Signal Forward Current Transfer Ratio (hfe @ 20 MC)

Small Signal Short Circuit Forward Transfer Current Ratio Cut-Off Frequency (Fab)

Gain Bandwidth Product (ft)

Collector Capacitance (Cob)

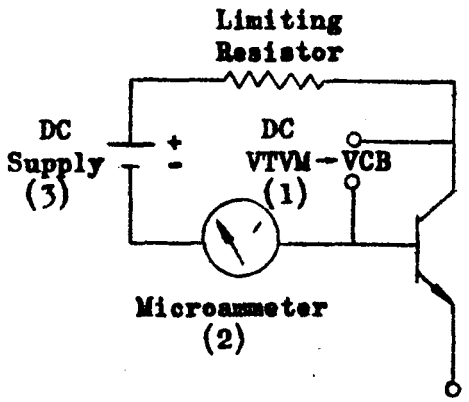
Noise Figure (N.F.)

Rise, Fall and Storage Time Measurements

COLLECTOR-BASE CUT-OFF CURRENT (I_{CBO})

TEST PROCEDURE

The Collector-Base Cut-Off Current was measured with the specified reverse bias voltage applied to the collector-base junction with the emitter element open-circuited. The measurement was performed with a Baird-Atomic Inc., Model KP2H, Transistor Test Set. A simplified circuit diagram of the Test Set and auxiliary test equipment follows:



(1) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.
(2) Microammeter, Hewlett-Packard, Model 425A.
(3) DC Supply Section of the Baird-Atomic Inc. Transistor Test Set, Model KP2H.

The bias voltage (VCB) was slowly increased to its required level and the collector leakage current read directly with the series-connected microammeter.

COLLECTOR-BASE CUT-OFF CURRENT (I_{CBO})

TEST PROCEDURE (Continued)

If unstable ICBO readings were encountered, the collector leakage current measurements were recorded after a ten-second interval. Further, if the leakage current approached or exceeded its maximum specified value when slowly increasing the bias, the voltage was immediately removed to avoid damaging the Transistor under test.

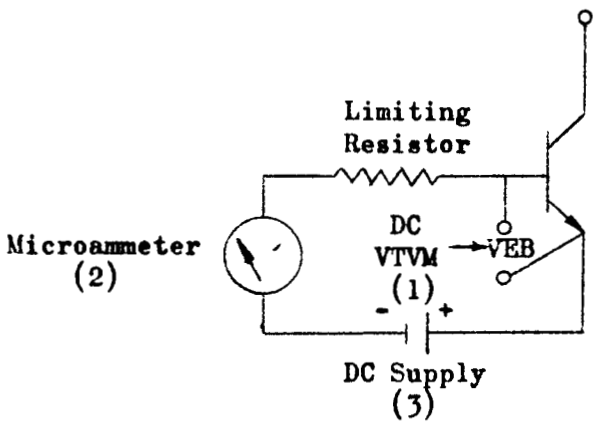
Where possible, voltage correlation of VCB versus ICBO was recorded on the leakage failures to further clarify the data. The leakage current (ICBO) recorded at room ambient conditions was not to exceed the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data section of this report.

EMITTER-BASE CUT-OFF CURRENT (I_{EBO})

TEST PROCEDURE

The Emitter-Base Cut-Off Current was measured with the required reverse bias voltage applied to the emitter-base junction with the collector element open-circuited. The measurement was performed with a Baird-Atomic Inc., Model KP2H, Transistor Test Set. A simplified circuit diagram of the Test Set and auxiliary test equipment follows:



(1) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.
(2) Microammeter, Hewlett-Packard, Model 425A.
(3) DC Supply Section of the Baird-Atomic Inc. Transistor Test Set, Model KP2H.

The bias voltage (VEB) was slowly increased to its required level and the emitter leakage current read directly with a series-connected microammeter.

EMITTER-BASE CUT-OFF CURRENT (I_{EBO})

TEST PROCEDURE (Continued)

If unstable IEBO readings were encountered, the emitter leakage currents were recorded after a ten-second stabilization period.

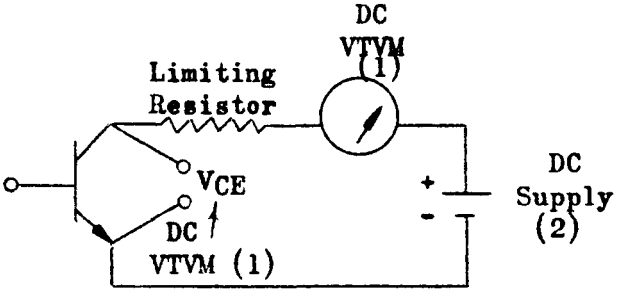
Where possible, voltage correlation of VEB versus IEBO was recorded on the leakage failures to further clarify the data. The leakage current (IEBO) recorded at room ambient conditions was not to exceed the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data section of this report.

COLLECTOR REVERSE CURRENT (I_{CEO})

TEST PROCEDURE

The Collector Reverse Current was measured with the specified bias voltage applied to the Collector and Emitter elements and with the base element open-circuited. A simplified circuit diagram and test equipment follows:



(1) DC Vacuum Tube Voltmeter, Hewlett-Packard Model 412A

(2) Constant Voltage Power Supply, Electronic Measurements Co. Model 212A

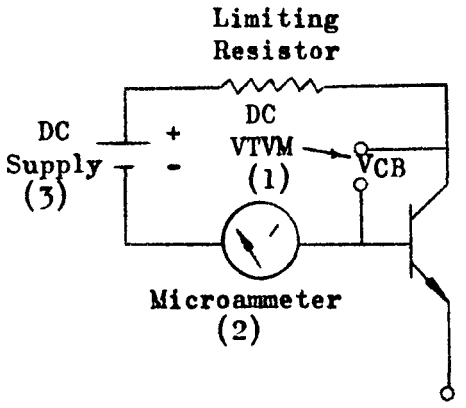
The bias voltage was slowly increased until the Collector-Emitter voltage (VCE) reached the required value. The Collector Current (IC) was then recorded as the Collector Reverse Current (ICEO). When measured at room ambient conditions, the reverse current was not to exceed the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data section of this report.

COLLECTOR-BASE BREAKDOWN VOLTAGE (BV_{CBO})

TEST PROCEDURE

The Collector-Base Breakdown Voltage was determined by reverse biasing the collector to base junction with the emitter element open-circuited. This was accomplished utilizing the Baird-Atomic Inc., Model KP2H, Transistor Test Set. The Test Set Parameter Selector Switch was set in the ICO position, since the circuit configuration conformed with that of the ICO Parameter Measurement. A simplified circuit diagram of the test set and auxiliary test equipment follows:



(1) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.
(2) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 425A.
(3) DC Supply Section of the Baird-Atomic Inc. Transistor Test Set, Model KP2H.

The bias voltage was slowly increased until the leakage or reverse current reached the specified value. The voltage VCB was then recorded as the breakdown voltage. The measured breakdown voltage was not to be less than the specified limit.

However, if the breakdown voltage was greater than the specified limit before reaching the required current, the bias voltage was immediately removed to avoid damaging the test specimen. Conditions such as these

COLLECTOR-BASE BREAKDOWN VOLTAGE (BV_{CBO})

TEST PROCEDURE (Continued)

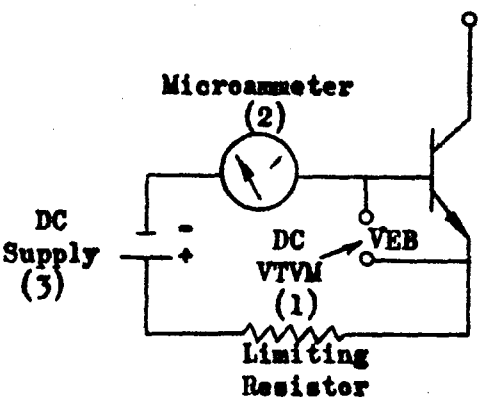
were identified in the Test Data as breakdown voltages (BVCBO) greater than the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

EMITTER-BASE BREAKDOWN VOLTAGE (BV_{EBO})

TEST PROCEDURE

The Emitter-Base Breakdown Voltage was determined by reverse biasing the emitter-base junction with the collector element open circuited. This was accomplished utilizing the Baird-Atomic Inc. Transistor Test Set, Model KP2H and auxiliary test equipment. The Test Set Parameter Selector Switch was set in the IEO position, since the circuit configuration conformed with that of the IEO Parameter Measurement. A simplified circuit diagram of the Test Set and auxiliary test equipment follows:



(1) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.
(2) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 425A.
(3) DC Supply Section of the Baird-Atomic Inc. Transistor Test Set, Model KP2H.

The bias voltage was slowly increased until the leakage or reverse current reached the specified value. The voltage VEB was recorded as the breakdown voltage. The measured breakdown voltage was not to be less than the specified limit.

EMITTER BASE BREAKDOWN VOLTAGE (BV_{EBO})

TEST PROCEDURE (Continued)

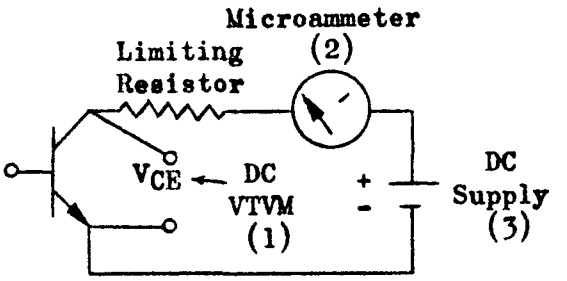
However, if the breakdown voltage was greater than the specified limit before reaching the specified reverse current, the bias voltage was immediately removed to avoid damaging the test specimen. Conditions such as these were identified in the Test Data as breakdown voltages (BVEBO) greater than the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

COLLECTOR-EMITTER BREAKDOWN VOLTAGE (BV_{CEO})

TEST PROCEDURE

The Collector-Emitter Breakdown Voltage (BVCEO) was measured with a bias voltage applied to the collector-emitter elements with the base open circuited. This was accomplished utilizing the Baird-Atomic Inc. Transistor Test Set, Model KP2H and auxiliary test equipment. A simplified circuit diagram of the test set and auxiliary test equipment follows:



(1) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.
(2) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 425A.
(3) DC Supply Section of the Baird-Atomic Inc. Transistor Test Set, Model KP2H

The bias voltage was slowly increased until IC reached the specified value. The voltage, VCE, was then recorded as the Collector-Emitter Breakdown Voltage (BVCEO). The measured breakdown voltage was not to be less than the specified limit.

COLLECTOR-EMITTER BREAKDOWN VOLTAGE (BV_{CEO})

TEST PROCEDURE (Continued)

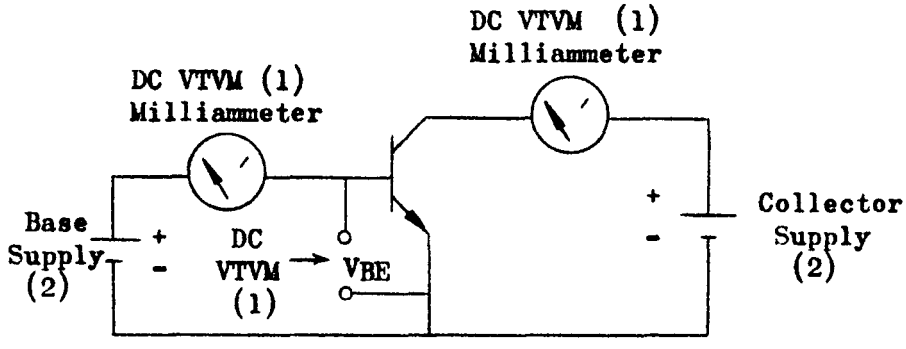
However, if the breakdown voltage was greater than the specified limit before reaching the required reverse current, the bias voltage was immediately removed to avoid damaging the test specimen. Conditions such as these were identified in the Test Data as breakdown voltages (BVCEO) greater than the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

BASE EMITTER VOLTAGE (VBE)

TEST PROCEDURE

The Base-Emitter Voltage (VBE) was measured utilizing a Baird-Atomic Inc. Transistor Test Set, Model KP2H and auxiliary test equipment. A simplified circuit diagram of the Test Set and auxiliary test equipment follows:



(1) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.
(2) DC Supply Section of the Baird-Atomic, Inc. Transistor Test Set, Model KP2H.

The bias voltages were slowly increased until the collector and base currents reached their specified values. When these conditions were established, the Base-Emitter Voltage (VBE) was measured and recorded.

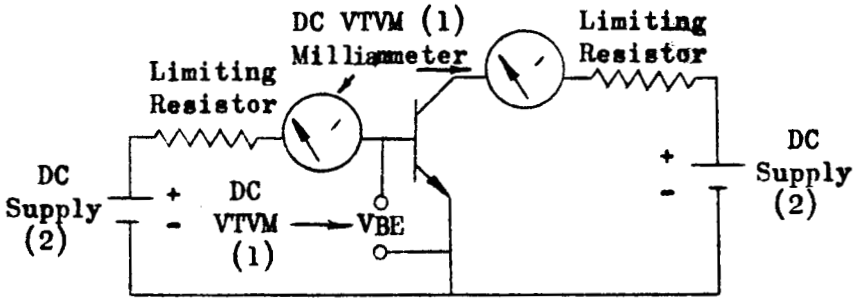
The Base-Emitter Voltage (VBE) was not to exceed the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

BASE EMITTER SATURATION VOLTAGE (VBE SAT)

TEST PROCEDURE

The base to emitter voltage was measured with the bias conditions established as required. This was accomplished utilizing the Baird-Atomic Inc. Transistor Test Set, Model KP2H. A simplified circuit diagram of the Test Set and auxiliary test equipment follows:



(1) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.
(2) DC Supply Section of the Baird-Atomic, Inc. Transistor Test Set, Model KP2H.

The bias voltages were slowly increased until the collector and base currents reached their specified values. When these conditions were established, the base to emitter voltage (VBE) was measured and recorded as VBE SAT.

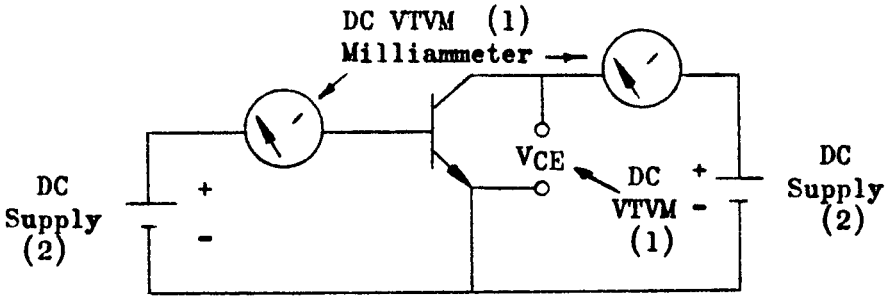
The base to emitter voltage (VBE SAT) was not to exceed the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

COLLECTOR EMITTER SATURATION VOLTAGE (VCE SAT)

TEST PROCEDURE

The collector to emitter voltage was measured with the bias conditions established as required. This was accomplished utilizing the Baird-Atomic, Inc. Transistor Test Set, Model KP2H. A simplified circuit diagram of the Test Set and auxiliary test equipment follows:



(1) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.
(2) DC Supply Section of the Baird-Atomic, Inc. Transistor Test Set, Model KP2H

The bias voltages were slowly increased until the collector and base currents reached their specified values. When these conditions were established, the collector-emitter voltage (VCE) was measured and recorded as VCE SAT.

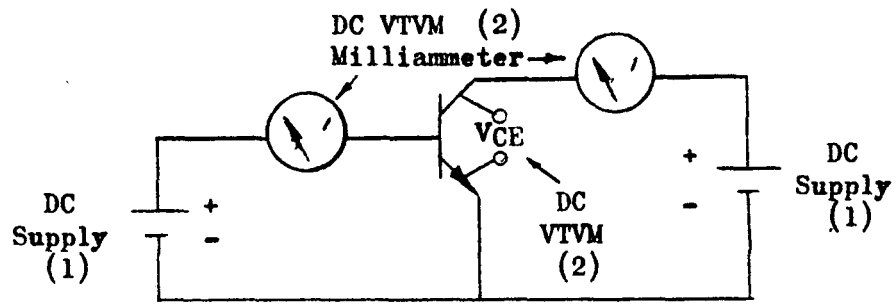
The Collector Saturation Voltage (VCE SAT) was not to exceed the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

DC COLLECTOR SATURATION RESISTANCE (R_{CS})

TEST PROCEDURE

The Saturation Resistance was determined by first measuring the saturation voltage. The Collector Saturation Voltage was measured with the required bias conditions applied. A simplified diagram of the test circuit and auxiliary test equipment follows:



(1) Constant Current Supply, Electronic Measurements Co., Model 612A.
(2) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.

The bias voltages were increased until the Collector and Base currents reached their specified values. When these conditions were established, the Collector-Emitter Voltage was measured and recorded as VCE SAT. The Collector Saturation Resistance was determined by using the following formula:

$$R_{CS} = \frac{(VCE\ SAT)}{I_C}$$

Where:

R_{CS} = Saturation Resistance

VCE_{SAT} = Saturation Voltage

I_C = Current where VCE_{SAT} was measured

DC COLLECTOR SATURATION RESISTANCE (R_{CS})

TEST PROCEDURE (Continued)

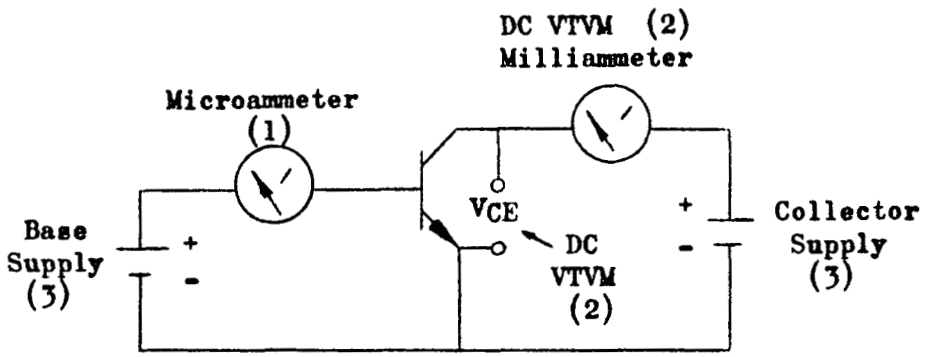
The Collector Saturation Resistance was not to exceed the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

STATIC FORWARD CURRENT TRANSFER RATIO (DC h_{FE})

TEST PROCEDURE

The Static Forward Current Transfer Ratio (DC h_{FE}) was determined utilizing the DC Supply Section of the Baird Atomic, Inc. Transistor Test Set, Model KP2H. A simplified circuit diagram of the Test Set and auxiliary equipment follows:



(1) Microammeter, Hewlett-Packard, Model 425A.
(2) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.
(3) DC Supply Sections of the Baird-Atomic, Inc. Transistor Test Set, Model KP2H.

With the proper collector to emitter voltage VCE applied, the base drive was slowly increased until the collector current (IC) reached the required value. With these conditions established, the base current (IB) was measured on the series connected microammeter. These values were recorded and inserted in the following expression:

$$h_{FE} = \frac{I_C}{I_B}$$

STATIC FORWARD CURRENT TRANSFER RATIO (DC h_{FE})

TEST PROCEDURE (Continued)

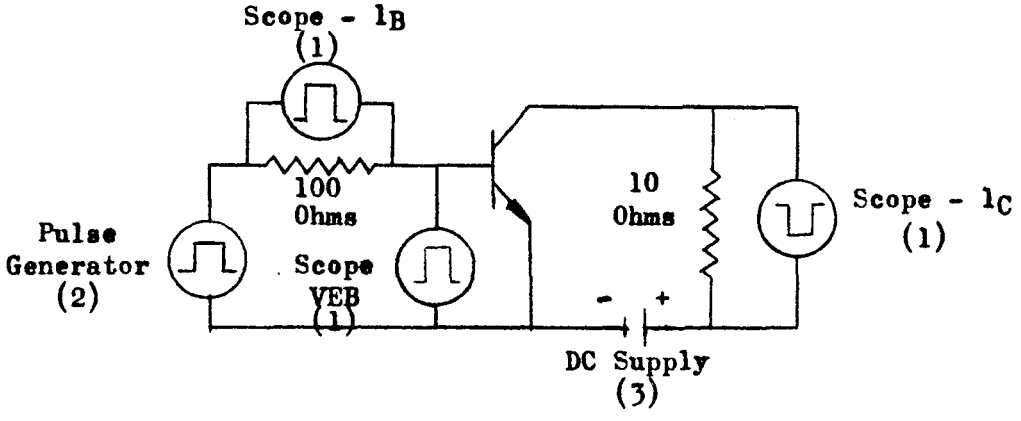
The Static Forward Current Transfer Ratio (DC hFE) was not to be less than the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

EMITTER-BASE SATURATION, PULSE, (VEB SAT)

TEST PROCEDURE

The Emitter-Base Voltage was measured with the specified bias voltage applied. The measurements were performed under pulse conditions utilizing a test circuit similar to the simplified circuit diagram and test equipment as follows:



(1) Oscilloscope, Tektronix, Model 545A.
(2) Pulse Generator, Electro-Pulse, Inc., Model 3450C.
(3) DC Supply, Sorenson & Co., Inc., Model T50-1.5.

Primarily, the input pulse was adjusted to the required pulse width and duty cycle. Simultaneously, the pulse amplitude and bias voltage were adjusted so that under pulsating conditions the collector current IC reached the required value (which was monitored as a voltage drop across the 10 ohm collector resistor) and the base current IB reached the required value (which was monitored as a voltage drop across the 100 ohm base resistor).

EMITTER-BASE SATURATION, PULSE, (VEB SAT)

TEST PROCEDURE (Continued)

With the above conditions established, the emitter to base voltage VEB was observed on the oscilloscope and the value recorded as the Emitter-Base Saturation Voltage (VEB SAT).

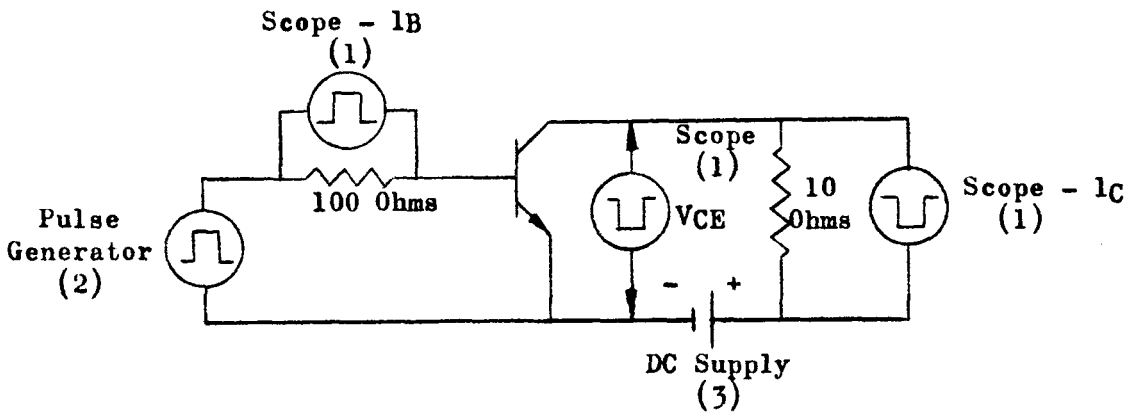
The Emitter-Base Saturation Voltage was not to exceed the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

COLLECTOR SATURATION, PULSE, (VCE SAT)

TEST PROCEDURE

The collector to emitter voltage was measured with the specified bias voltage applied. The measurements were performed under pulse conditions utilizing a test circuit similar to the simplified circuit diagram and test equipment as follows:



(1) Oscilloscope, Tektronix, Model 545A.
(2) Pulse Generator, Electro-Pulse, Inc., Model 3450C.
(3) DC Supply, Sorenson & Co., Inc., Model T50-1.5.

Primarily, the input pulse was adjusted to the required pulse width and duty cycle. Simultaneously, the pulse amplitude and bias voltage were adjusted so that under pulsating conditions the collector current IC reached the required value (which was monitored as a voltage drop across the 10 ohm collector resistor) and the base current IB reached the required value (which was monitored as a voltage drop across the 100 ohm base resistor).

COLLECTOR SATURATION, PULSE, (VCE SAT)

TEST PROCEDURE (Continued)

With the above conditions established, the collector to emitter voltage (VCE) was observed on the Oscilloscope and the value recorded as the Collector Saturation Voltage (VCE SAT).

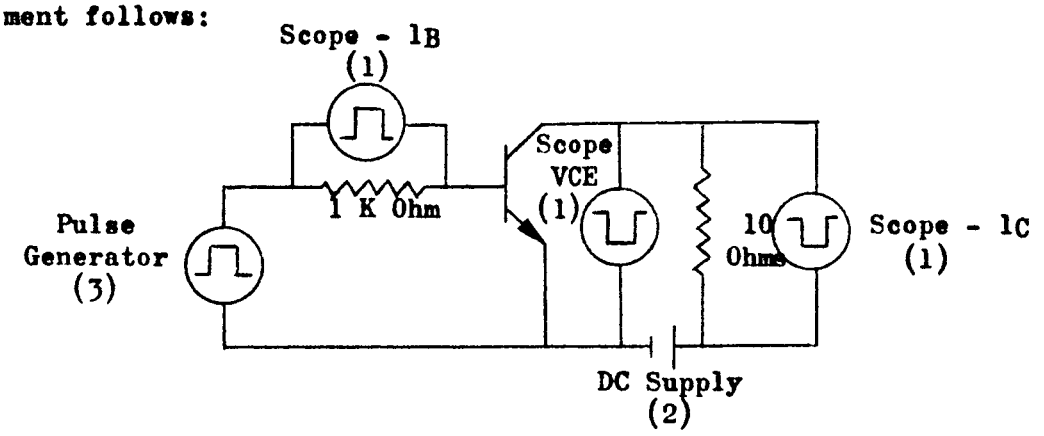
The Collector Saturation Voltage (VCE SAT) was not to exceed the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

STATIC FORWARD CURRENT TRANSFER RATIO (PULSE h_{FE})

TEST PROCEDURE

The Static Forward Current Transfer Ratio was measured under pulse conditions. A simplified circuit diagram and auxiliary test equipment follows:



(1) Oscilloscope, Tektronix, Model 545A.
(2) DC Supply, Sorenson & Co., Inc., Model T50-1.5.
(3) Pulse Generator, Electro-Pulse, Inc., Model 3450C.

Primarily, the input pulse was adjusted to the required pulse width and duty cycle. Simultaneously, the pulse amplitude and bias voltage VCE were adjusted so that under pulsating conditions (pulse DC level at maximum amplitude) VCE reached the required value at the specified collector current IC (which was monitored as a voltage drop across the 10 ohm collector resistor). The voltage drop across the 1K base resistor was then observed and measured on an oscilloscope. The voltage drop in volts was analagous to the base current IB in milliamperes since a 1K base resistor was selected to perform the measurement.

STATIC FORWARD CURRENT TRANSFER RATIO (PULSE h_{FE})

TEST PROCEDURE (Continued)

The base and collector currents were substituted into the following expression:

$$h_{FE} = \frac{I_C}{I_B}$$

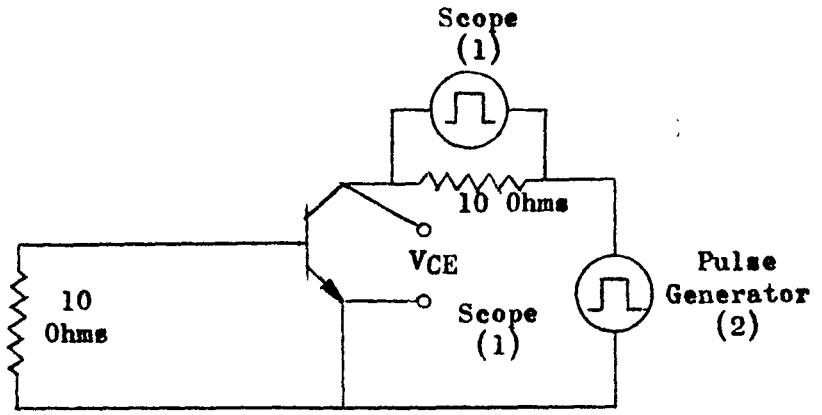
The Static Forward Current Transfer Ratio (Pulse hFE) measurements were to be within the limits as specified.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

LOWER LIMITING VOLTAGE (LVCER)

TEST PROCEDURE

The Lower Limiting Voltage was determined on each Transistor test specimen. A simplified circuit diagram of the test circuit and auxiliary test equipment follows:



(1) Oscilloscope, Tektronix, Model 545A.
(2) Pulse Generator, Electro-Pulse, Inc., Model 3450C.

Primarily, the input pulse was adjusted to the required pulse width and duty cycle.

The Pulse Generator was interconnected between the collector and emitter elements and a 10 ohm resistor inserted between the base and emitter to bias the Transistor virtually at cut-off. The pulse amplitude was slowly increased until the collector current or reverse current reached the specified value and the voltage VCE recorded as the Lower Limiting Voltage. The resulting collector current was determined utilizing the voltage drop across the 10 ohm collector resistor (a proportionate voltage drop across 10 ohms).

LOWER LIMITING VOLTAGE (LVCER)

TEST PROCEDURE (Continued)

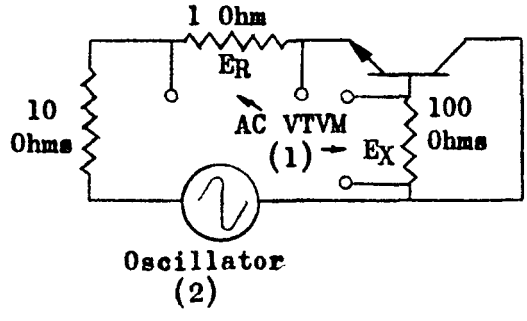
The measured Lower Limiting Voltage (LVCER) was not to exceed the specified limit. However, if the Lower Limiting Voltage was greater than the specified limit before reaching the required reverse current, the pulse amplitude was immediately decreased to avoid damaging the test specimen. A condition such as this was identified in the test data as a Lower Limiting Voltage (LVCER) greater than the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

FORWARD CURRENT TRANSFER RATIO (h_{fb})

TEST PROCEDURE

In order to increase the accuracy of the determination of hfb (Forward Current Transfer Ratio) the measurement was performed in terms of the hybrid parameter 1 + hfb (or 1 - Alpha). Since hfb was greater than 0.9, the accuracy with which the parameter was measured increased by a factor of 10, utilizing the quantity of 1 + hfb as the directly measured parameter. A simplified circuit diagram of the Test Set and auxiliary test equipment follows:



(The DC bias supplies were omitted to simplify the above diagram.)

(1) AC Vacuum Tube Voltmeter, Hewlett-Packard, Model 400H.
(2) Oscillator, Hewlett-Packard, Model 200CD.

Note: The DC bias conditions of VCB and IE were measured on DC Vacuum Tube Voltmeters (2) Hewlett-Packard, Model 412A.

The bias voltage was slowly increased until the Collector-Base Voltage (VCB) and the Emitter Current (IE) reached their required values. With the proper DC bias established, an AC signal component was introduced and its amplitude increased until a voltage drop of 10 millivolts (ER) was

FORWARD CURRENT TRANSFER RATIO (h_{fb})

TEST PROCEDURE (Continued)

observed across the 1 ohm emitter resistor. The meter switch was then transferred to its "E_X" position and the voltage drop across the 100 ohm base resistor measured (AC component). These values were recorded and inserted in the following expression:

$$1 + h_{fb} = \frac{E_X}{E_R} \times .01$$

Therefore: $$h_{fb} = 1 - \frac{E_X}{E_R} \times .01$$

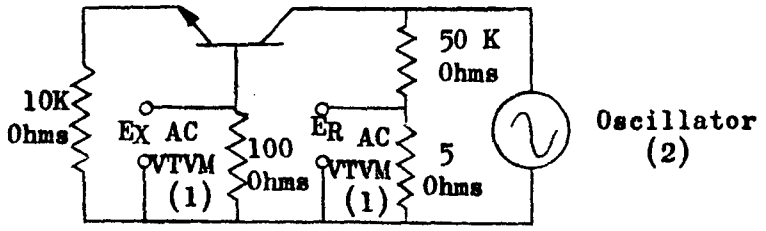
The calculated values of hfb were to be within the range of specified values.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

SMALL SIGNAL OPEN CIRCUIT OUTPUT ADMITTANCE (h_{ob})

TEST PROCEDURE

The Output admittance (hob) was determined with the signal input AC theoretically open circuited and with the Transistor connected in the common base configuration. This was accomplished utilizing the Baird-Atomic Inc. Transistor Test Set, Model KP2H and auxiliary test equipment. A simplified circuit diagram of the Test Set and auxiliary test equipment follows:



(The DC bias supplies were omitted to simplify the above diagram)

(1) AC Vacuum Tube Voltmeter, Hewlett-Packard, Model 400H.
(2) Oscillator, Hewlett-Packard, Model 200CD.

Note: The DC bias conditions of VCB and IE were measured on DC Vacuum Tube Voltmeters (2), Hewlett-Packard, Model 412A.

The bias voltage was slowly increased until the Collector-Base Voltage (VCB) and the Emitter Current (IE) reached their required values. With the proper DC bias conditions established, a 1KC signal component was introduced and its amplitude increased until a 10 millivolt drop (E_R) was observed across the 5 ohm collector resistor. The meter switch was

SMALL SIGNAL OPEN CIRCUIT OUTPUT ADMITTANCE (h_{ob})

TEST PROCEDURE (Continued)

then transferred to its "E_X" position and the voltage drop across the 100 ohm base resistor measured (AC component). These values were recorded and inserted into the following expression:

$$h_{ob} = \frac{E_X}{E_R} \times 1 \text{ umho}$$

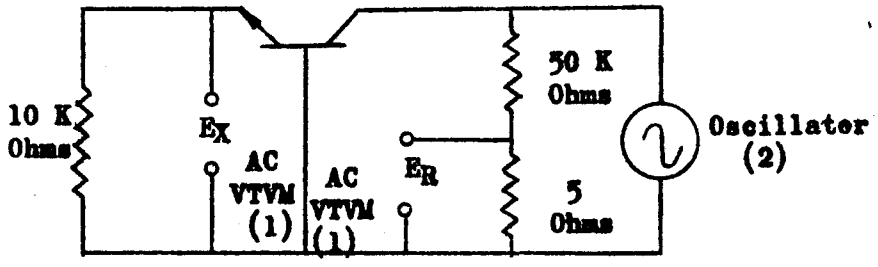
The calculated values of hob were to be within the range of specified limits.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

SMALL SIGNAL OPEN CIRCUIT REVERSE TRANSFER VOLTAGE RATIO (hrb)

TEST PROCEDURE

The voltage feedback ratio (hrb) was determined with the input AC theoretically open circuited and with the Transistor connected in the common base configuration. This was accomplished utilizing the Baird-Atomic Inc. Transistor Test Set, Model KP2H and auxiliary test equipment. A simplified circuit diagram of the Test Set and auxiliary test equipment follows:



(The DC bias supplies were omitted to simplify the above diagram)

(1) AC Vacuum Tube Voltmeter, Hewlett-Packard, Model 400H.
(2) Oscillator, Hewlett-Packard, Model 200CD.

Note: The DC bias conditions of VCB and IE were measured on DC Vacuum Tube Voltmeters (2), Hewlett-Packard, Model 412A.

The bias voltage was slowly increased until the Collector-Base Voltage (VCB) and the Emitter Current (IE) reached their required values. With the proper DC bias conditions established, a 1KC signal component was introduced and its amplitude increased until a 10 millivolt drop (E_R) was observed across the 5 ohm collector resistor. The meter switch was

SMALL SIGNAL OPEN CIRCUIT
REVERSE TRANSFER VOLTAGE RATIO (hrb)

TEST PROCEDURE (Continued)

then transferred to its "E_X" position and the voltage drop across the 10,000 ohm emitter resistor measured (AC component). These values were recorded and inserted into the following expression:

$$h_{rb} = \frac{E_X}{E_R} \times 10^{-4}$$

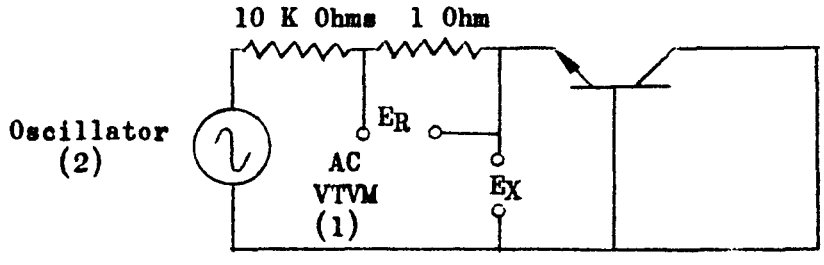
The calculated values of hrb were to be within the range of specified limits.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

SMALL SIGNAL SHORT CIRCUIT INPUT IMPEDANCE (h_{ib})

TEST PROCEDURE

The Input Impedance, base to emitter, was measured with the Transistor connected in the common base configuration with the output AC theoretically short circuited. This was accomplished utilizing the Baird-Atomic Inc. Transistor Test Set, Model KP2H and auxiliary test equipment. A simplified circuit diagram of the Test Set and auxiliary test equipment follows:



(The DC bias supplies were omitted to simplify the above diagram.)

(1) AC Vacuum Tube Voltmeter, Hewlett-Packard, Model 400H.
(2) Oscillator, Hewlett-Packard, Model 200CD.

Note: The DC bias conditions of VCB and IE were measured on DC Vacuum Tube Voltmeters (2), Hewlett-Packard, Model 412A.

The bias voltage was slowy increased until the Collector-Base Voltage (VCB) and the Emitter Current (IE) reached their required values. With the proper DC bias conditions established, a 1KC signal was introduced and its amplitude increased until a 10 millivolt drop (E_R) was observed across the 1 ohm emitter resistor. The meter switch was then transferred

SMALL SIGNAL SHORT CIRCUIT INPUT IMPEDANCE (h_{ib})

TEST PROCEDURE (Continued)

to its "E_X" position and the voltage VEB measured (AC component). These values were recorded and inserted into the following expression:

$$h_{ib} = \frac{E_X}{E_R} \text{ ohms}$$

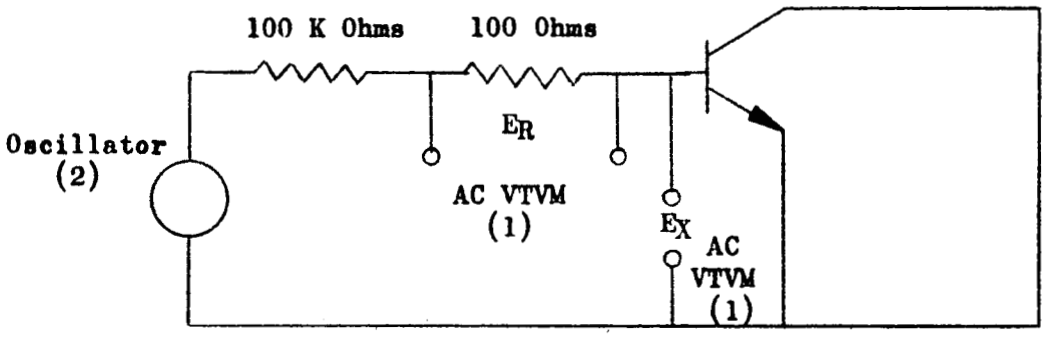
The Input Impedance was to be within the range of limits as specified.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

SMALL SIGNAL SHORT CIRCUIT INPUT IMPEDANCE (hie)

TEST PROCEDURE

The Input Impedance, base to emitter, was measured with the Transistor Connected in the common emitter configuration with the output AC theoretically short circuited. This was accomplished utilizing the Baird-Atomic Inc. Transistor Test Set, Model KP2H and auxiliary test equipment. A simplified circuit diagram of the Test Set and auxiliary test equipment follows:



(The DC bias supplies were omitted to simplify the above diagram.)

(1) AC Vacuum Tube Voltmeter, Hewlett-Packard, Model 400H.
(2) Oscillator, Hewlett-Packard, Model 200CD.

Note: The DC bias conditions of VCE and IC were measured on DC Vacuum Tube Voltmeters (2), Hewlett-Packard, Model 412A.

The bias voltage was slowly increased until the Collector-Emitter Voltage (VCE) and the Collector Current (IC) reached their required values. With the proper DC bias conditions established, a 1KC signal was introduced and its amplitude increased until a 10 millivolt drop (E_R) was observed across the 100 ohm baseresistor. The meter switch

SMALL SIGNAL SHORT CIRCUIT INPUT IMPEDANCE (hie)

TEST PROCEDURE (Continued)

was then transferred to its "E_X" position and the voltage VEB measured (AC component). These values were recorded and inserted into the following expression:

$$hie = \frac{E_X}{E_R} \quad \text{ohms}$$

The Input Impedance was to be within the range of limits as specified.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

STORAGE LIFE TEST

TEST PROCEDURE

Ten of the submitted Transistors and Diodes, per type, were inserted in a Storage Life Test fixture fabricated by Associated Testing Laboratories, Inc. The fixture in turn was placed within the Model LHH-30 High Temperature Test Chamber manufactured by Associated Testing Laboratories, Inc.

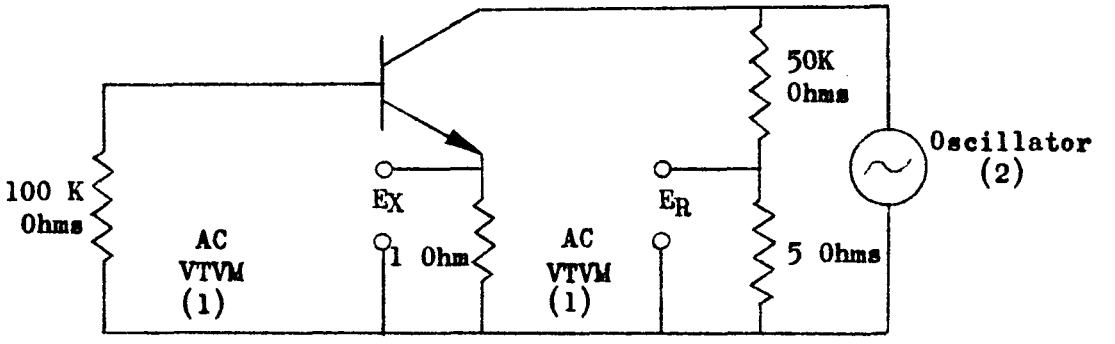
The internal temperature of the chamber was raised to and maintained at +150°C (302°F) for a period of 2000 hours.

The Transistors and Diodes were removed from the chamber at the completion of 50, 100, 250, 500, 1000, 1500 and 2000 hours of testing for end point measurements. The measurements performed are listed in detail on the individual Storage Life Test data sheets.

SMALL SIGNAL OPEN CIRCUIT OUTPUT ADMITTANCE (hoe)

TEST PROCEDURE

The output admittance (hoe) was determined with the signal input AC theoretically open circuited and with the Transistor connected in the common emitter configuration. This was accomplished utilizing the Baird-Atomic Inc. Transistor Test Set, Model KP2H and auxiliary test equipment. A simplified circuit diagram of the Test Set and auxiliary test equipment follows:



(The DC bias supplies were omitted to simplify the above diagram.)

(1) AC Vacuum Tube Voltmeter, Hewlett-Packard, Model 400H.
(2) Oscillator, Hewlett-Packard, Model 200CD.

Note: The DC bias conditions of VCE and IC were measured on DC Vacuum Tube Voltmeters (2), Hewlett-Packard, Model 412A.

The bias voltage was slowly increased until the Collector-Emitter Voltage (VCE) and the Collector Current (IC) reached their required values. With the proper DC bias conditions established, a 1KC signal component was introduced and its amplitude increased until a 10 millivolt drop (E_R) was observed across the 5 ohm collector resistor. The meter switch was

SMALL SIGNAL OPEN CIRCUIT OUTPUT ADMITTANCE (hoe)

TEST PROCEDURE (Continued)

then transferred to its "E_X" position and the voltage drop across the one ohm emitter resistor measured (AC component). These values were recorded and inserted into the following expression:

$$hoe = \frac{E_X}{E_R} \times 1 \text{ umho}$$

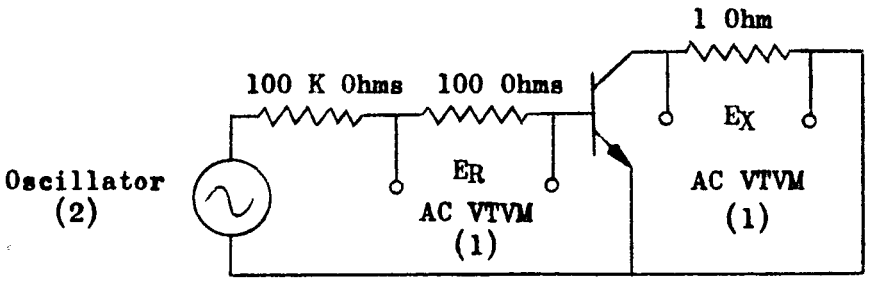
The calculated values of hoe were to be within the range of specified limits.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

SMALL SIGNAL SHORT CIRCUIT FORWARD CURRENT TRANSFER RATIO (h_{fe} @ 1KC)

TEST PROCEDURE

The Forward Current Transfer Ratio (hfe) was measured with the output AC theoretically short circuited and with the Transistor connected in the common emitter configuration. This was accomplished utilizing the Baird-Atomic Inc. Transistor Test Set, Model KP2H and auxiliary test equipment. A simplified circuit diagram of the Test Set and auxiliary equipment follows:



(The DC bias supplies were omitted to simplify the above diagram.)

(1) AC Vacuum Tube Voltmeter, Hewlett-Packard, Model 400H.
(2) Oscillator, Hewlett-Packard, Model 200CD.

Note: The DC bias conditions of VCB and IE were measured on DC Vacuum Tube Voltmeters (2), Hewlett-Packard, Model 412A.

The bias voltage was slowly increased until the Collector-Base Voltage (VCB) and the Emitter Current (IE) reached their required values. With the proper DC bias established, a 1KC signal component was introduced and its amplitude increased until a 10 millivolt voltage drop (E_R) was observed across the 100 ohm base resistor. The meter switch was then transferred to its "E_X" position and the voltage drop across the 1 ohm

SMALL SIGNAL SHORT CIRCUIT FORWARD CURRENT TRANSFER RATIO (hfe @ 1KC)

TEST PROCEDURE (Continued)

collector was measured (AC component). These values were recorded and inserted into the following expression:

$$h_{fe} = \frac{E_X}{E_R} \times 10$$

The Forward Current Transfer Ratio (hfe) was not to be less than the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

SMALL SIGNAL FORWARD CURRENT TRANSFER RATIO (hfe @ 1 MC)

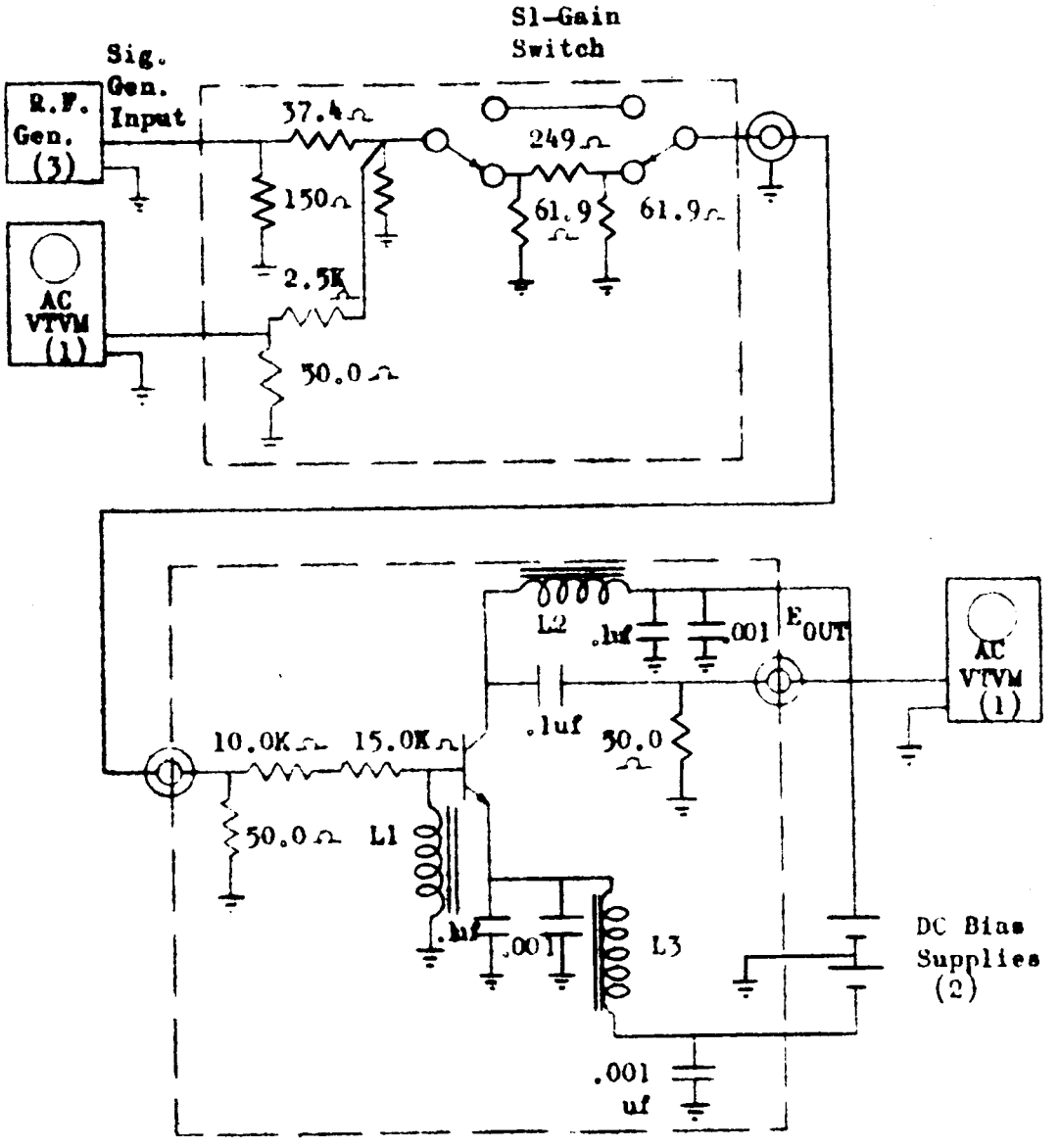
TEST PROCEDURE

The common emitter forward current transfer ratio (hfe) was measured on each transistor test specimen at the test frequency of 1.0 megacycle. This was accomplished utilizing an especially fabricated instrument as shown in the circuit diagram on the following page.

The necessary external bias supplies were connected (grounded base biasing), an RF signal generator was connected to the "Sig Gen Input" and a wide band AC vacuum tube voltmeter was connected to the "EIN" and "GND" terminals.

The DC bias supplies were slowly increased until the specified conditions of the collector-emitter voltage (VCE) and the emitter current (IE) were obtained. With these conditions established, a 1.0 megacycle signal component was introduced and slowly increased until a meter reading of 3.16 millivolts was observed across the "EIN" terminals and "GND" (full scale deflection on the 3 millivolt range). The vacuum tube voltmeter was then transferred to the "Eout" and "GND" terminals and the AC output signal read directly in terms of common emitter current gain on the 3 millivolt range, 0 - 10 or 0 - 100, depending upon the setting of the gain switch "S1".

The current gain when measured at a test frequency of 1.0 megacycle was not to be less than the specified limit.



(1) AC Vacuum Tube Voltmeter, Hewlett-Packard, Model 400H.
(2) DC Supplies, Opad Electric Company, Model KM75B.
(3) R.F. Generator, General Radio, Model 1390B.

1.0 MC TRANSISTOR CURRENT GAIN TEST SET

1 MC Test Set, Dynatran Electronics Corporation, Serial No. 610401

SMALL SIGNAL FORWARD CURRENT TRANSFER RATIO (hfe @ 20 MC)

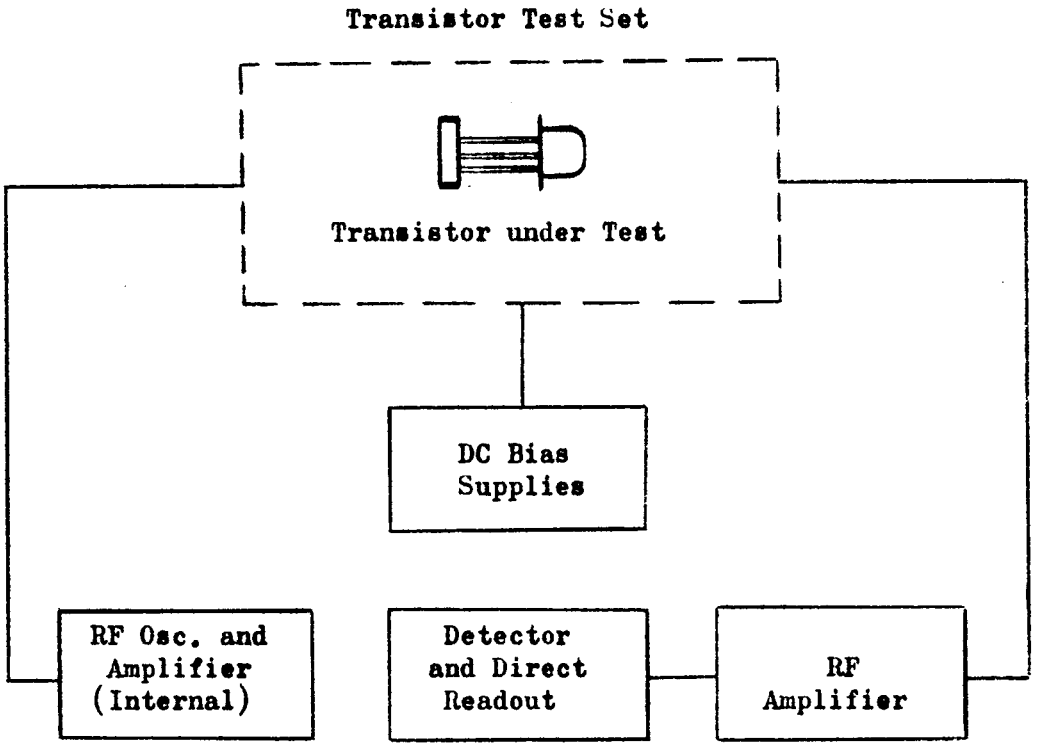
TEST PROCEDURE

The common emitter forward current transfer ratio (hfe) was measured on each transistor test specimen at the test frequency of 20 megacycles. This was accomplished utilizing an especially fabricated instrument. A block diagram illustrating its basic method of operation is shown on the following page.

The internal DC bias supplies were slowly increased until the specified conditions of the collector-emitter voltage (VCE) and collector current (IC) were obtained. Since the overall gain of the RF oscillator and amplifier stage was fixed, the common emitter current gain was observed immediately after establishing the bias conditions. Direct readout was accomplished by inserting the specimen in a fixed gain amplifier, the output of which was detected and presented in terms of common emitter gain.

The current gain when measured at the test frequency of 20 megacycles was not to be less than the specified limit.

hfe 20 MC Test Set



Dynatran, Model No. 610591

Associated Testing Laboratories, Inc.

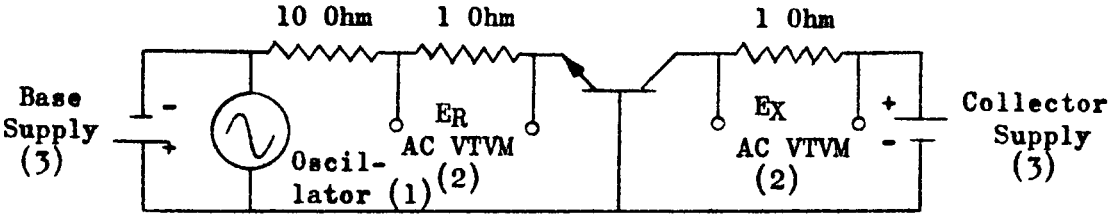
Wayne, New Jersey Winter Park, Florida

Burlington, Massachusetts

SMALL SIGNAL SHORT CIRCUIT FORWARD TRANSFER CURRENT RATIO CUT-OFF FREQUENCY (Fab)

TEST PROCEDURE

The measurement was performed on the Baird-Atomic Inc., Model KP2H Transistor Test Set. This was accomplished utilizing the common base current gain (hfb) function of the Transistor Test Set. A simplified circuit diagram of the Test Set and auxiliary test equipment follows;



(1) Oscillator, Hewlett-Packard, Model 200CD.
(2) AC Vacuum Tube Voltmeter, Hewlett-Packard, Model 400H.
(3) DC Supply Sections of the Baird-Atomic Inc. Transistor Test Set, Model KP2H.

Primarily, the bias voltages were slowly increased until the collector emitter voltage (VCE) and the collector current (IC) reached their required values.

The oscillator frequency was then increased until the output voltage "EX" was equal to .707 of the input voltage "ER". When these conditions were established, the frequency was recorded as Fab.

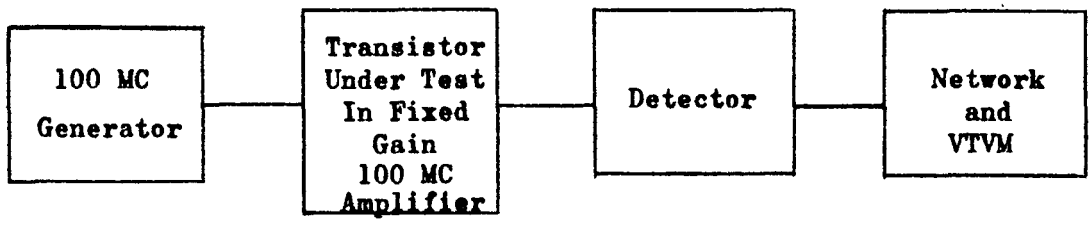
The Cut-Off Frequency was to be a value greater than the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

GAIN BANDWIDTH PRODUCT (f_t)

TEST PROCEDURE

The Gain Bandwidth Product (f_t), the product of the grounded emitter current gain at a specified frequency, multiplied by this frequency, was determined by utilizing a specially fabricated test set. A simplified block diagram of the test set follows:



f_t measured utilizing a Dynatran Electronics Inc. Test Set, Model 1818

The measurement was performed within the test set by measuring the current gain at the required test frequency. This current gain component was applied to a series network which introduced the necessary multiplication factor, allowing the parameter (f_t) to be read directly on the integral vacuum tube voltmeter.

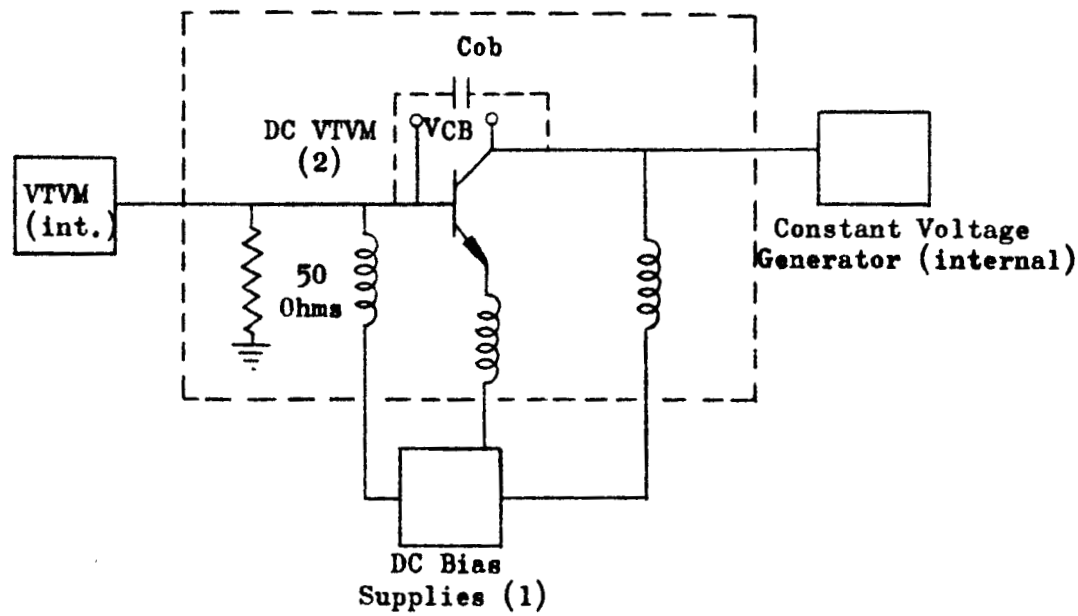
When measured at room ambient conditions, the Gain Bandwidth Product was not to be less than the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

COLLECTOR CAPACITANCE (C_{ob})

TEST PROCEDURE

The output collector to base capacitance, including the strap capacitance of the Transistor leads and case, was measured utilizing a Dynatran Electronics Corp. Transistor Test Set, Model 1827.1. A simplified block diagram of the Test Set and auxiliary test equipment follows:



(1) DC Supply Section of the Baird-Atomic Inc. Transistor Test Set, Model KP2H.
(2) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.

The measurement was performed at the required test frequency by sampling the current flow through the equivalent capacitor (capacitor across the collector and base junctions), since the current IB is theoretically proportional to the capacitance (Cob). The current IB

COLLECTOR CAPACITANCE (C_{ob})

TEST PROCEDURE (Continued)

was measured in terms of the voltage drop across the 50 ohm base resistor, which in turn, was read directly on a Vacuum Tube Voltmeter calibrated for Cob presentation.

The proper DC bias conditions as required and AC component voltages were applied to the Transistor under test with the emitter open circuited to the AC component. The Collector Capacitance (Cob) measurements were then recorded.

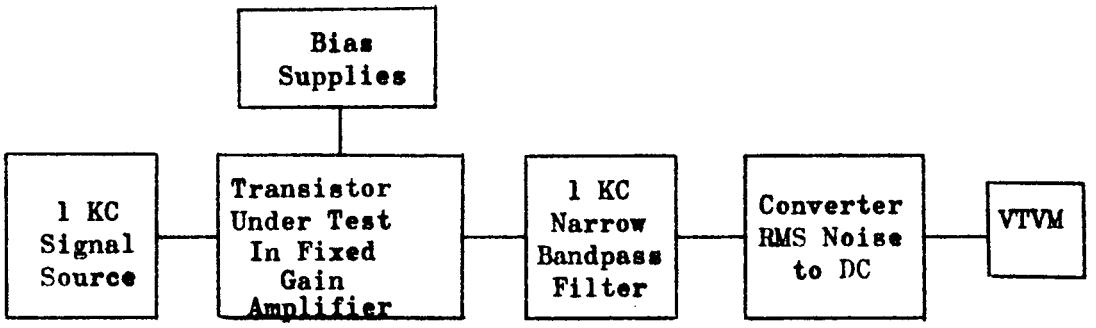
The collector to base capacitance was not to exceed the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

NOISE FIGURE (N.F.)

TEST PROCEDURE

The ratio of the total noise power at the output of the Transistor to that component of noise output due to the thermal noise in the source was measured on a noise tester (Transistor Noise Analyzer, Quan-Tech Laboratories Model 310). A simplified block diagram of the instrument follows:



Since the Noise Figure increases substantially with increasing emitter current and collector voltage, the collector-base bias voltage and the emitter current were critically adjusted to each of their required values. The noise output was then recorded in microamperes DC as observed on the Vacuum Tube Voltmeter. This was converted to Noise Figure by using a nomograph supplied with the test set, which related thermal noise in Rg (500 ohms) at room ambient temperature to the output noise of the Transistor Amplifier, as compensated for filter bandwidth. Since the current gain (B) of each Transistor was different the Gain was automatically corrected by the AGC System in the Test Unit.

The Noise Figure was not to exceed the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

RISE, FALL AND STORAGE TIME MEASUREMENTS

TEST PROCEDURE

Primarily, the pulse generator was adjusted to yield the specified pulse width and duty cycle. With these conditions established, the base current (I_B) and the collector current (I_C) were adjusted to their required values. The rise, fall and storage time characteristics were then measured.

A simplified circuit diagram of the switching modules and auxiliary test equipment utilized are shown on the following pages.

For clarity of definition, the time measurement characteristics observed were the following:

A. Rise Time

The time duration during which the amplitude of the leading edge of the output pulse increased from 10% to 90% of its maximum amplitude.

B. Storage Time

The time delay between the opening of the base circuit and the pulse decay of the collector circuit (10% down on the trailing edge of the output pulse).

C. Fall Time

The time duration during which the amplitude of the trailing edge decreased from 90% to 10% of the maximum amplitude.

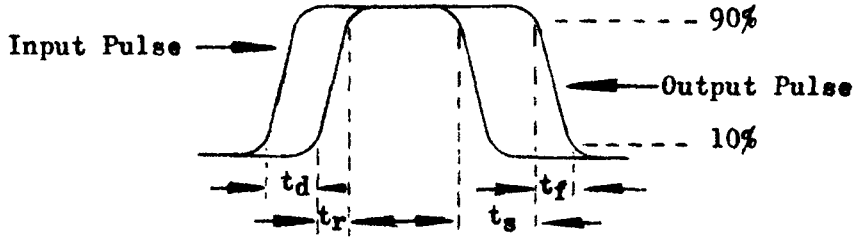
RISE, FALL AND STORAGE TIME MEASUREMENTS

TEST PROCEDURE (Continued)

D. Storage plus Fall Time

The time delay between the opening of the base circuit and the pulse decay of the collector circuit (10% down on the trailing edge of the output pulse) plus the time duration during which the amplitude of the trailing edge decreased from 90% to 10% of the maximum amplitude.

For further explanation, a pictorial representation of pulse definition follows:

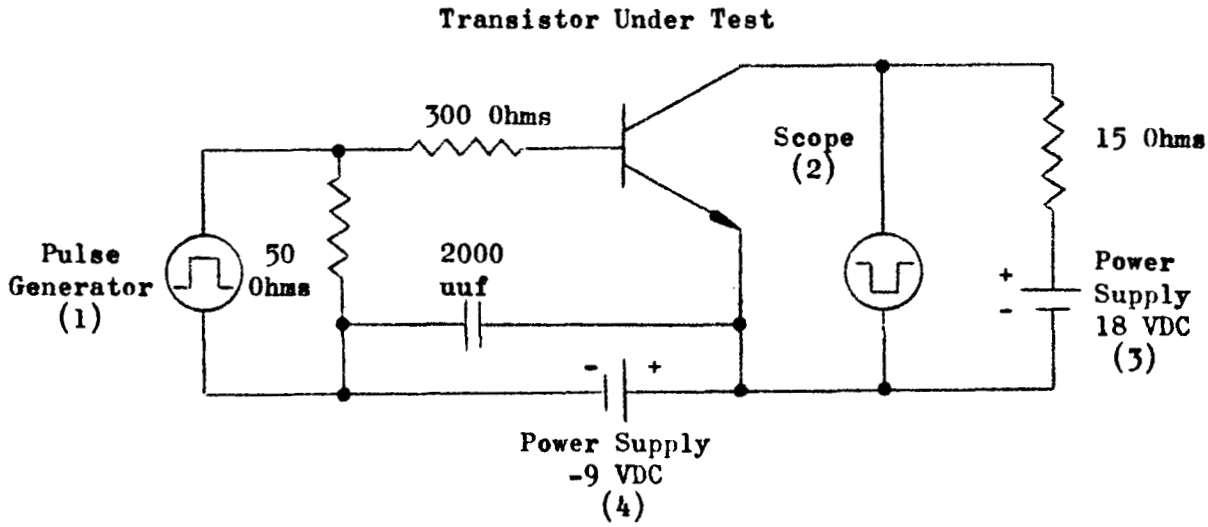


For specific bias test conditions required and for specified parameter limits, see the Original Test Data section of this report.

All measured values for the switching parameters were to be within the range of specified limits.

SWITCHING TIME TEST CIRCUITRY

(2N1650)



(1) Pulse Generator, Electro-Pulse, Model 3450C

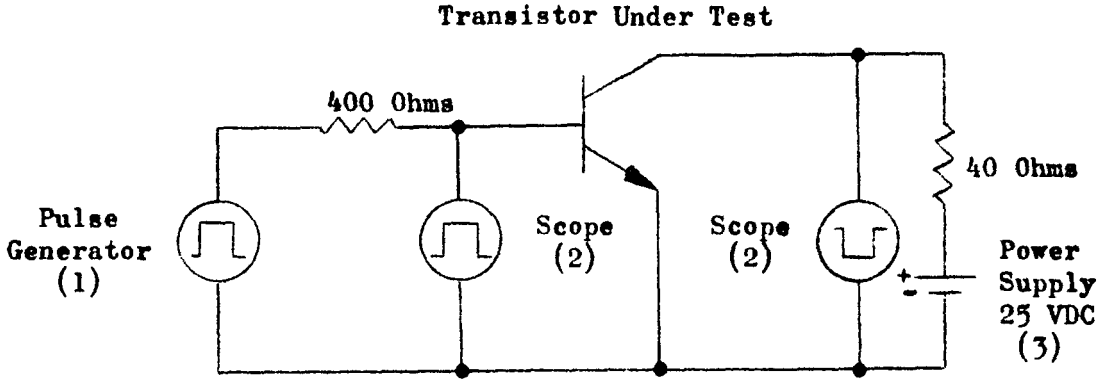
(2) Oscilloscope, Tektronix, Model 545

(3) Power Supply (Constant Voltage), Electronic Measurements, Inc. Model 214AL

(4) Power Supply (Constant Voltage), Electronic Measurements, Inc. Model 212AL

SWITCHING TIME TEST CIRCUITRY

(2N547 - 2N1116)



(1) Pulse Generator, Electro-Pulse, Model 3450C

(2) Oscilloscope, Tektronix, Model 545

(3) Power Supply (Constant Voltage), Electronic Measurements, Inc. Model 214AL

Report No. G231-2890

SECTION II

Diode Test Parameter Measurement Procedures

Forward Voltage Drop or Forward Current (VF)

Reverse Current or Saturation Voltage (IR)

Zener Voltage (VZ)

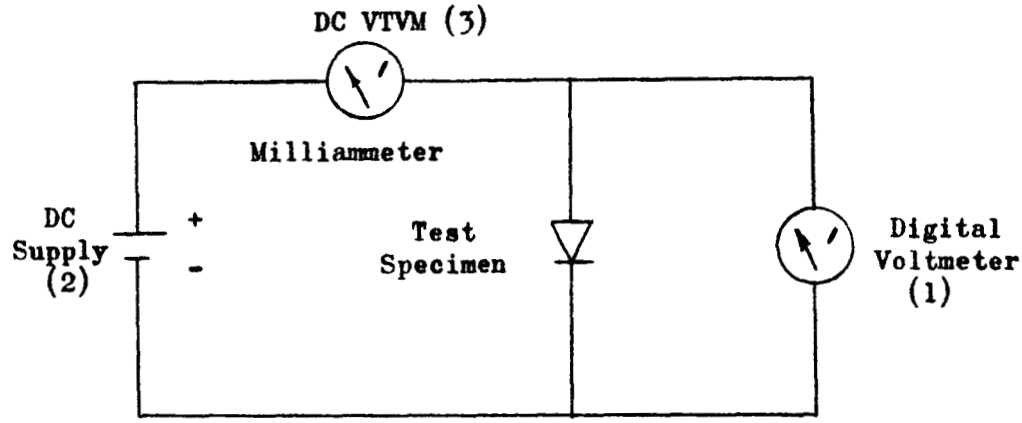
Dynamic Impedance (ZZ)

Reverse Recovery Time

FORWARD VOLTAGE DROP OR FORWARD CURRENT (VF)

TEST PROCEDURE

The Diode Forward Voltage Drop (VF) was measured on each test specimen utilizing a forward voltage test circuit and auxiliary test equipment. A simplified diagram of the test circuit and auxiliary test equipment follows:



(1) Digital Voltmeter, Cubic Corp., Model V-51.
(2) Constant Current Supply, Quan-Tech, Model 151B.
(3) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.

Primarily, the bias voltage was slowly increased until the required Forward Current was indicated on the series connected milliammeter. This was accomplished during a five second interval. With this condition established, the Forward Voltage Drop across the Diode was measured with a DC Digital Voltmeter and the value was recorded.

When performing Forward Current, it should be noted that the forward bias voltage was slowly increased to its required value and noted on the digital voltmeter. The resulting forward current was then measured on the milliammeter and recorded as the Forward Current.

FORWARD VOLTAGE DROP OR FORWARD CURRENT (VF)

TEST PROCEDURE (Continued)

It should be noted that prior to conducting the test, the DC Vacuum Tube Voltmeter (milliammeter section) was calibrated to read the required forward current within ± 1%.

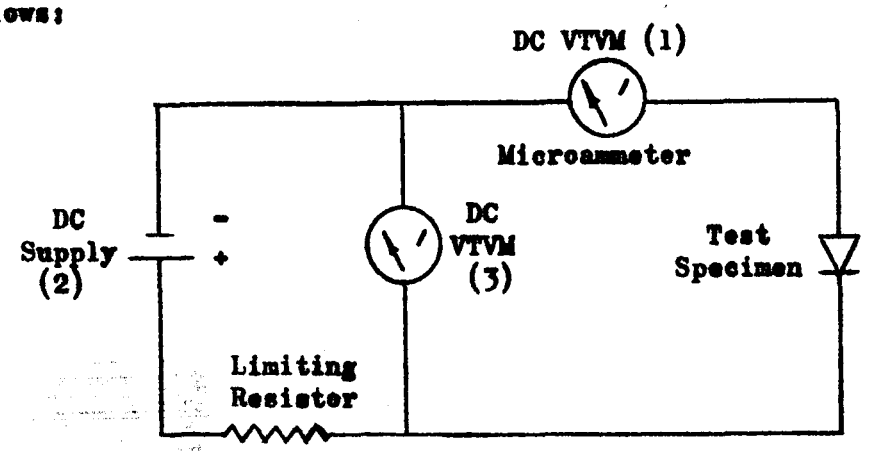
The Forward Voltage Drop was not to exceed the specified limit. The Forward Current was not to be less than the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

REVERSE CURRENT OR SATURATION VOLTAGE (IR)

TEST PROCEDURE

The Reverse Current (IR) was measured on each Diode submitted, utilizing a reverse current test circuit and auxiliary test equipment. A simplified diagram of the test circuit and auxiliary test equipment follows:



(1) DC Microammeter, Hewlett-Packard, Model 425A.
(2) DC Power Supply, Lambda Electric Co. Model 50.
(3) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.

Primarily, the impressed reverse bias voltage across the Diode was slowly increased from zero to the required voltage level during a five second interval. The Reverse Current was then read directly with the series connected microammeter.

When performing Saturation Voltage, it should be noted that as the reverse bias voltage was applied, the resulting reverse current was continuously monitored on the microammeter. When the reverse current reached its required value, the voltage was then recorded as the Saturation Voltage.

REVERSE CURRENT OR SATURATION VOLTAGE (IR)

TEST PROCEDURE (Continued)

Further, it should be noted that in the above Test Procedures, while the reverse bias was being applied, if the test diode was observed to draw an excessive amount of current (shorting condition), the voltage was immediately removed to avoid further damage to the test specimen.

The recorded values for reverse current were not to exceed the specified limit.

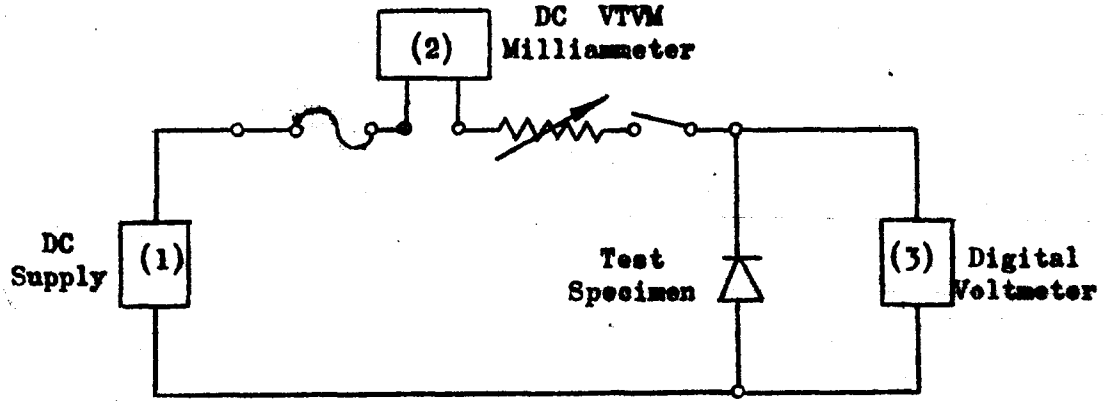
The recorded values for saturation voltage were not to be less than the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

ZENER VOLTAGE (VZ)

TEST PROCEDURE

The Zener Voltage (VZ) was measured on each test specimen utilizing a zener voltage test circuit and auxiliary test equipment. A simplified diagram of the test circuit and auxiliary test equipment follows:



(1) Constant Current Supply, Quan-Tech Model 151B.
(2) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.
(3) Digital Voltmeter, Cubic Corp., Model V-51.

Primarily, the bias voltage was slowly increased until the required Zener Current (IZ) was indicated on the series connected milliammeter. The corresponding Zener Voltage developed across the Diode was then measured on the digital voltmeter. All Diodes remained connected into the test circuit until no significant variation of the characteristic being measured was observed on the DC digital voltmeter.

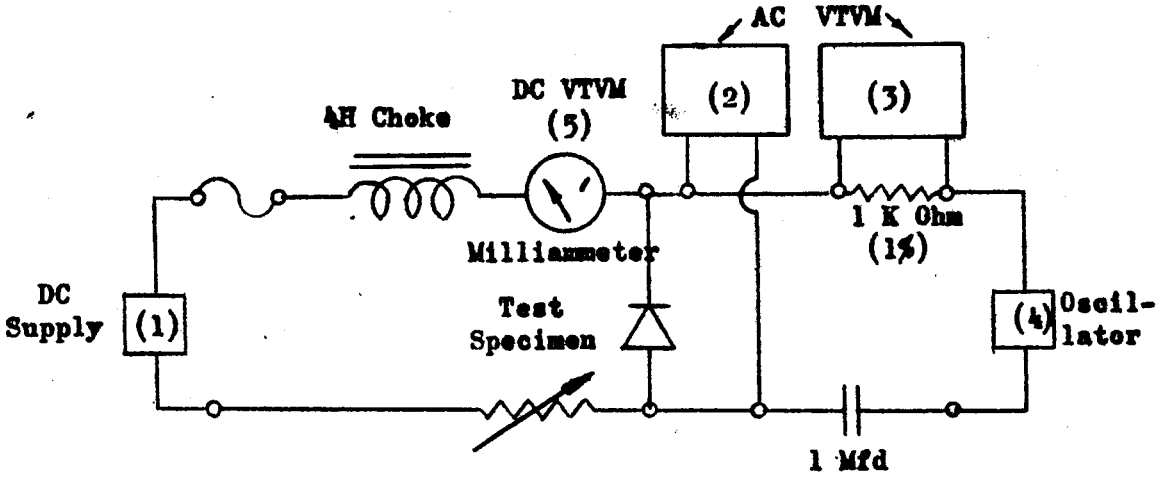
The Zener Voltage measurements recorded were to be within the range of the specified limits.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

DYNAMIC IMPEDANCE (ZZ)

TEST PROCEDURE

The Dynamic Impedance (ZZ) was measured on each test specimen utilizing a dynamic impedance test circuit and auxiliary test equipment. A simplified diagram of the test circuit and auxiliary test equipment follows:



(1) DC Power Supply, Sorenson & Co., Inc., Model T50-1.5.
(2) AC Voltmeter, Hewlett-Packard, Model 400H.
(3) AC Voltmeter, Hewlett-Packard, Model 400D.
(4) Wide Range Oscillator, Hewlett-Packard, Model 202C.
(5) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.

The Dynamic Impedance was determined by measuring the AC Voltage (E_p) developed across the Diode when operating with a 60 cycle AC Zener Current super-imposed on the Zener Test Current (IZ). The amplitude of the AC Current (rms) was 10% of the specified DC Zener Test Current (IZ) and was measured as a voltage drop across a 1000 ohm, 1%, precision resistor. The Dynamic Impedance was then calculated using the following formula:

$$ZZ\ (Ohms) = \frac{E_p\ (AC\ Volts)}{IZ\ (maAc)}$$

The Dynamic Impedance calculated was not to exceed the specified limit.

For specific bias test conditions required and for specified parameter limits, see the Original Test Data Section of this report.

REVERSE RECOVERY TIME

TEST PROCEDURE

The Reverse Recovery Time was determined on each Diode test specimen utilizing a test module constructed in accordance with the JAN256 drawing. The circuit diagram and equipment list are shown on the following pages.

The test was performed in the following sequence. Primarily, the specified value of R_L was inserted into the test circuit and the system calibrated as follows:

Step 1: The specified bias voltages were applied to the appropriate input terminals.

Step 2: The Forward Current was adjusted to zero.

Step 3: The inverse voltage (E_b) was adjusted so that the meter read one-half of the specified voltage, less than one-half the clamp voltage of 3 volts.

Step 4: A ± 1% precision carbon resistor was placed in the test clips, the purpose being to establish a known current value indication on the oscilloscope with the vertical amplifier in DC mode of operation. The oscilloscope was then calibrated by observing this current display and the zero reference line. The oscilloscope vertical deflection amplifier was calibrated such that the specified back resistance was represented by a two centimeter deflection below the center line on the oscilloscope graticle. The resistor was removed from the test clips.

Step 5: A Diode was inserted into the test clips and the forward bias adjusted to the required value with the inverse voltage (E_b) approximately adjusted. The inverse voltage (E_b) was readjusted to allow for the forward voltage drop across the Diode under test.

Step 6: The input signal, a negative going square wave (of the required duty cycle), displaying rise and fall time characteristics as specified, was applied. The pulse was adjusted to its required peak to peak amplitude.

REVERSE RECOVERY TIME

TEST PROCEDURE (Continued)

Step 7: The rise time characteristics of both the oscilloscope and cathode follower were observed and found to be less than 0.05 microsecond. Further, the total load shunt capacitance was determined by placing a ten micromicrofarad capacitor in the test clips with R_L removed to form a voltage divider with C_L. The value calculated was approximately ten micromicrofarads.

Step 8: The reverse recovery time was then measured on the oscilloscope utilizing the appropriate sweep rate.

Both the reverse resistance and the reverse recover time when measured at room temperature with circuit parameters as specified, were to be within the range of specified limits.

SECTION III

Transistor and Diode Environmental Test Procedures

Thermal Shock Test

Lead Fatigue Test

Temperature Cycling Test

Case Leakage Test

Mechanical Shock Test

Vibration Variable Frequency Test

Altitude Test

GENERAL

The following comprise the environmental test procedures utilized in this program. It should be noted that in all cases, reference is made to the Transistors submitted for testing. However, in the case of Diodes, when it is necessary for them to undergo a like environment, the particular test method with reference to Transistors, shall also apply to Diodes.

THERMAL SHOCK TEST

TEST PROCEDURE

The Transistors were subjected alternately to five cycles of immersion in tap water at 0°C (+32°F) and +100°C (+212°F) for a period of not less than five seconds and fifteen seconds respectively. The low temperature bath was maintained at the specified temperatures with the addition of ice cubes. The high temperature bath was heated by a hot plate and maintained at the boiling state. Further, the quantities of bath solutions were of sufficient volume to maintain the required temperatures upon immersion of the test specimens.

The transfer of the Transistors from the high and low temperature baths was accomplished utilizing a wire screen basket and the transfer was not to exceed a ten second interval.

At the completion of the test, the Transistors were examined for evidence of physical damage.

LEAD FATIGUE TEST

TEST PROCEDURE

Of the Transistor test groups subjected to lead fatigue, five Transistors of each test group were subjected to the lead pull. Each lead was subjected to a total of three 90° arcs of the case. A lead weight was attached to each lead by means of a three inch flexible cable and an alligator type clip. The weight applied to each lead, including the cable and alligator clip was 16.05 ounces (455 grams). Each lead was restricted by means of a round-tip, needle-nose plier so that the bend occurred 3/32 ±1/32 inch from the Transistor housing. All arcs on a single lead were performed in the same direction and in the same plane without torsion, to a position perpendicular to the pull axis and back to the normal position.

Two leads of each Transistor were subjected to the Lead Fatigue Test. In addition, the leads were chosen so that each Transistor was subjected to two of the three possible lead combinations (base and emitter, base and collector, emitter and collector).

TEMPERATURE CYCLING TEST

The Temperature Cycling Test was performed using two separate chambers. Each chamber was stabilized at the temperature extreme, -65°C (-85°F) with non-controlled humidity and +90°C (+194°F) with relative humidity controlled at 95% respectively. The High Temperature Humidity Chamber was governed by means of a two-pen, cam controller. The test specimens, mounted on heat resistant fixtures suitable for the high and low temperature environments, were then placed within the chamber and maintained at the low temperature extreme for a period of twelve hours. Upon completion of this portion of the temperature cycle, the test specimens were removed from the low temperature and allowed to remain at a room temperature condition of +25°C (+77°F) for a period of fifteen minutes, at the completion of which they were placed within the chamber maintained at the high temperature extreme for a period of twelve hours.

Thermal equilibrium in all cases was established by three successive thermocouple readings fifteen minutes apart and within ±2°C of each other. The above operation comprised one complete cycle of temperature cycling. A total of five 24-hour cycles was performed.

At the completion of the test, the Transistors were examined for evidence of physical damage.

CASE LEAKAGE TEST

TEST PROCEDURE

The Transistors, while mounted to the test fixtures, were placed within a High Pressure Chamber containing a solution of 99.5 parts by weight of demineralized water and 0.5 parts by weight of liquid detergent. The internal pressure of the test chamber was then increased to 75 psig for a period of three hours. At the completion of this period, the Transistors were removed from the Pressure Chamber, rinsed in running tap water and allowed to dry in a chamber maintained at +40°C (+104°F) for three hours. The Transistors were then subjected to a visual examination, after which the end point measurements as specified, were performed.

MECHANICAL SHOCK TEST

TEST PROCEDURE

The test fixture containing the Transistors was securely fastened to the table of the Shock Machine.

The Transistors were subjected to five shocks in each direction along each of the three principle axes for a total of thirty shocks. Each shock had a 1500 g peak amplitude and a duration of 0.5 millisecond, with a wave shape approximating one-half sine wave.

Prior to testing, the Shock Machine was calibrated to yield the specified shock pulse. The shock pulses were generated by raising the table of the Shock Machine to a pre-calibrated height and then permitting the table to free fall. The fall was terminated upon impact of the underside of the shock table on the steel arresting bed. There was no excitation voltage applied to the Transistors during the Shock Test.

After each shock, the Transistors were examined for physical damage after which the end point measurements, as specified, were performed.

VIBRATION VARIABLE FREQUENCY TEST

TEST PROCEDURE

The Transisters were securely inserted in the Vibration Test Fixture which, in turn, was rigidly mounted to the table of the vibration exciter. The units were then subjected to one forty-minute cycle of applied sine vibration in each of the three mutually perpendicular axes, a cycle consisting of a frequency sweep throughout the range of 20 cps to 2000 cps. Throughout the entire frequency sweep, the applied vibratory motion was maintained at 20 g or 0.125 inch da, whichever was the limiting factor.

Following the Vibration Testing, the test specimens were removed from the Vibration Test Fixture and examined for evidence of physical damage after which the end point measurements, as specified, were performed.

ALTITUDE TEST

TEST PROCEDURE

In order to perform the test under operating conditions, the Transistor test specimens were placed within the Altitude Chamber in their mating sockets.

For the required simulated altitudes, a Model A-4-L Altitude Chamber, manufactured by Associated Testing Laboratories, Inc. and a Kinney High Vacuum System, Model PW-600 with integral feed-throughs were utilized. Both altitude systems enabled the test operator to view the test specimens while under the simulated environment. For operating conditions, with the Model A-4-L Altitude Chamber, the cables interconnecting the test sockets with the Transistor test panel were exited through access ports in the chamber wall. With the Kinney High Vacuum System, the integral feed-throughs were utilized in the cabling interconnecting the test sockets with the Transistor test panel.

With the test set as described above, the internal pressure of the chamber was then reduced to the required value. When the required altitude environment was established, the Transistors were preconditioned for a ten minute interval, after which the collector-base leakage current (ICBO) was measured on each test specimen. The temperature prior to and during the Altitude Test was maintained at +25°C ±3°C.

After completing the ICBO parameter measurements, the internal pressure of the chamber was raised to room ambient. The Transistors were then removed from the Altitude Test Chamber and examined for evidence of physical damage after which the specified end point measurements were performed. (The altitude test levels were 3 mm, 0.17 mm, and 10^{-5} mm (or less) of mercury.

SECTION IV

2000 Hour Life Tests

a) Operational

b) Storage

Associated Testing Laboratories, Inc.

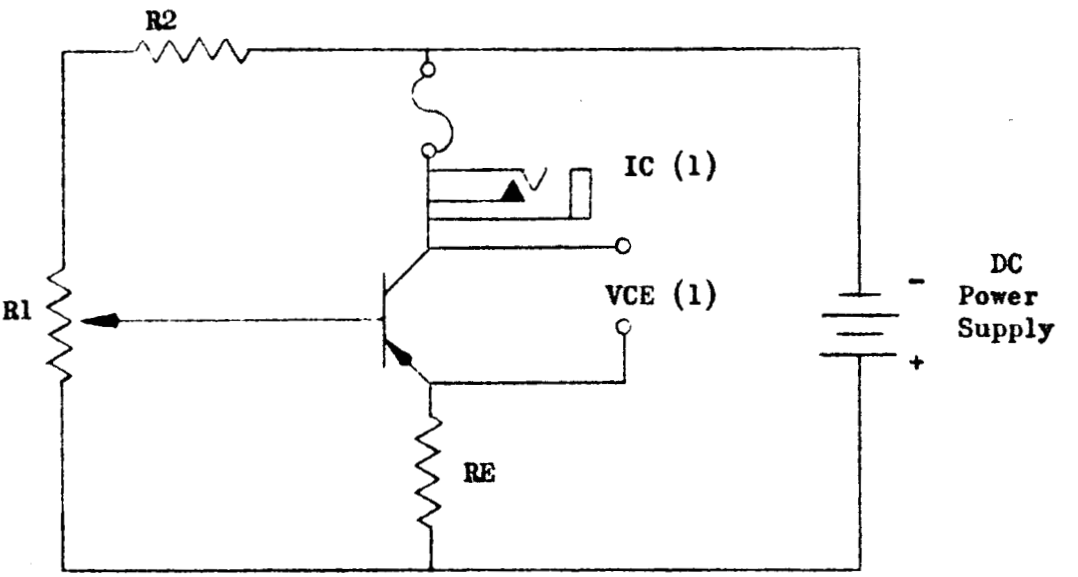
Wayne, New Jersey Winter Park, Florida

Burlington, Massachusetts

OPERATION LIFE TEST

TEST PROCEDURE

Ten Transistors, per type, were subjected to the 2000 Hour Operation Life Test. The Transistors were paralled and inserted into Life Test circuits fabricated by Associated Testing Laboratories, Inc. A simplified diagram of a typical Life Test circuit is shown below.



(1) DC Vacuum Tube Voltmeter, Hewlett-Packard, Model 412A.
(2) DC Supply, Opad Electric Co., Model RS20.

The Life Test modules were energized and the bias voltages were adjusted to yield the maximum power dissipation. The bias and test conditions are shown in the table on the following page.

The Transistors were removed from the Life Test circuits at the completion of 100, 250, 500, 1000, 1500 and 2000 hours of testing for end point measurements. The measurements performed are listed in detail on the individual Operation Life Test data sheets.

OPERATIONAL LIFE TEST CONDITIONS

Type	VCE (VDC)	IC (madc)	Pd (mw)	R_1 (ohms)	R_2 (ohms)	R_E (ohms)	Ambient Condition
NS117	16.0	25.0	400	50K	0	1.0K	TA = +25°C
2N328	15.4	25.0	385	50K	0	1.0K	TA = +25°C
2N718	25.0	20.0	500	50K	680	1.8K	TA = +25°C
2N335	15.0	10.0	150	50K	10K	1.5K	TA = +25°C
2N336	15.0	10.0	150	50K	10K	1.5K	TA = +25°C
2N119	15.0	10.0	150	50K	10K	1.5K	TA = +25°C
2N703	15.0	20.0	300	50K	0	1.0K	TA = +25°C
CK419	10.0	8.0	80	50K	0	2.7K	TA = +25°C
T1367	10.0	8.0	80	50K	0	2.7K	TA = +25°C
2N547	5.0	120	600	150	10	43.0	TA = +25°C
2N542	15.0	13.3	200	50K	10K	1.0K	TA = +25°C
2N1650	20.0	500	10.0 watts	50.0	10	10.0	Note 1
2N1116	60.0	33.3	2.0 watts	50K	10K	820	Note 2
2N1016	24.0	2.7	70.0 watts	50.0	5.0	5.0	Note 3

Note 1: 2N1650 - Test performed with Transistors placed within a constantly agitated Silicon oil bath (TC = 100 - 110°C).

Note 2: 2N1116 - Test performed in a High Temperature Associated Testing Laboratories, Inc. Chamber (TA = +68°C) with Transistors mounted on 3" X 3" X 1/16" aluminum heat sinks.

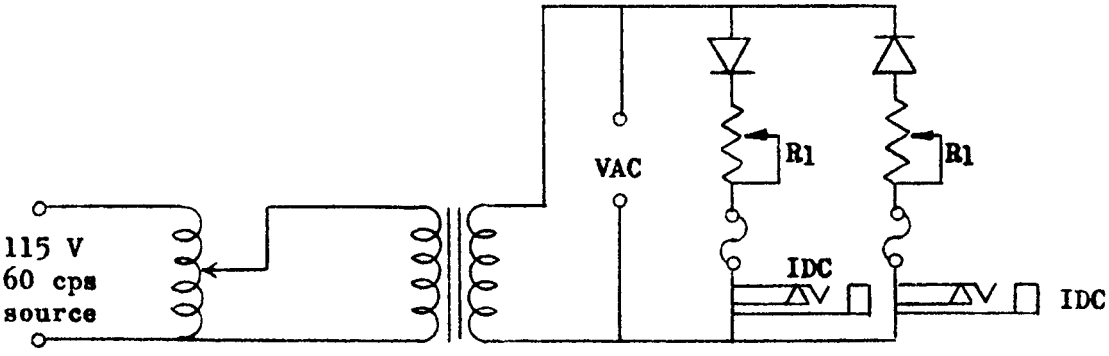
Note 3: 2N1016 - Life Test performed with TC = 90 - 100°C. The units were mounted on Wakefield heat sinks Model 5100 with 30cfm used to maintain case temperature.

OPERATION LIFE TEST

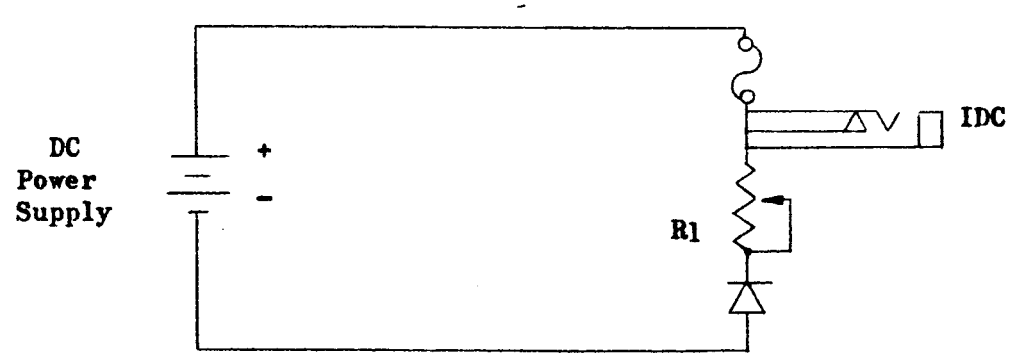
TEST PROCEDURE

Ten Diodes, per type, were subjected to the 2000 Hour Life Test. The Diodes were inserted into Life Test circuits fabricated by Associated Testing Laboratories, Inc. Simplified diagrams of the Life Test circuits are shown below.

Rectifier Diodes



Zener Diodes



OPERATION LIFE TEST

(continued)

TEST PROCEDURE (continued)

The Life Test modules were energized and the units were subjected to rated power. Rectifier Diodes were energized with an AC voltage whose peak value was equal to the P.I.V of the Diodes. Load resistor R1 was then adjusted until the maximum specified DC current was obtained. Alternate Diodes in the Life Test circuit were reversed so that no DC component would be present in the transformers.

The Zener Diodes were energized with a DC voltage. The DC current to produce the rated voltages was calculated using the nominal zener voltage rating. R1 was then adjusted until this current was obtained.

OPERATION LIFE TEST CONDITIONS

Type	VAC	IDC	VDC	Ambient Condition
1N461	17.7	90 ma	N/A	+25°C
1N461	17.7	60 ma	N/A	+25°C
1N482B	25.5	200 ma	N/A	+25°C
1N48313	49.5	200 ma	N/A	+25°C
1N540	283	250 ma	N/A	+25°C
1N347	71	1.0 amp.	N/A	+25°C
1N626	35.5	20 ma	N/A	+25°C
1N1612	35.5	5.0 amp.	N/A	+25°C
1N2069	141	750 ma	N/A	+25°C
UT267	283*	2 amp.*	N/A	+25°C
521B	280	12 amp.	N/A	+25°C
1N752A	N/A	71.5 ma	5.6	+25°C
1N702	N/A	77 ma	2.6	+25°C
314M18Z10	N/A	41.5 ma	18	+25°C
SV135	N/A	20.8 ma	12	+25°C
SV808	N/A	86 ma	8.75	+25°C

* Unit was to be run at 424 VAC and 3.0 amperes DC. However, they would not operate at these values. Spare units were used to evaluate the maximum current and voltage the units would withstand.

Associated Testing Laboratories, Inc.

Wayne, New Jersey Winter Park, Florida

Burlington, Massachusetts